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Title: Contact Resistance and Stability Assessment of Oxide-Based Thin Film Transistors

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This thesis focuses on two aspects of oxide-based thin-film transistors (TFTs), contact resistance and instability assessment.

First, determination of the contact resistance of indium tin oxide (ITO) on two wide-band gap semiconductors, zinc oxide (ZnO) and indium gallium oxide (IGO), is attempted and the effects of contact resistance on device performance is investigated. Both transistor and transfer length method (TLM) structures are used in the study and three material systems are employed: ZnO on SiO_2, ZnO on aluminum titanium oxide (ATO), and IGO on SiO_2. It is found that the measured resistance is not dominated by contact resistance effects. It is concluded that the device dimensions used in this study (i.e., gate lengths of 50 to 200 μm) are too large to yield an accurate estimate of the contact resistance, since it is so small.

Second, a methodology for assessing the stability of oxide-based TFTs is developed and implemented. This methodology involves constant voltage stressing over a maximum duration of 10^5 s (i.e., ~ 28 hours) and periodic evaluation of drain current-drain voltage and drain current-gate voltage characteristics during the stability test. This stability assessment strategy is first applied to three semiconducting materials: ZnO, zinc indium oxide (ZIO), and IGO, using thermal silicon oxide as the gate dielectric. Similar trends are observed for these device types. Relatively stable devices are obtained

after post-deposition annealing at a temperature of ~ 600 °C for ZnO and IGO TFTs, and ~ 400 °C for ZIO TFTs. The presence of instability in these devices, which is more pronounced at a lower annealing temperature, results in a positive shift in the turn-on voltage and clockwise hysteresis in the drain current-gate voltage transfer curve. Such an instability is attributed to electron trapping near the channel/insulator interface. The stability a ZnO TFT fabricated using a spin-coat synthesized aluminum phosphate (AlPO) as the gate dielectric is also investigated. The ZnO/AlPO TFT showed distinctively different stability trends. This device is observed to be very unstable with a negative shift in the turn-on voltage and counter-clockwise hysteresis in the drain current-gate voltage transfer curve. The mechanism for this instability is ascribed to insulator ion drift. It is shown that stable TFTs can be fabricated with oxide-based channel layers if a high quality insulator, such as thermal silicon dioxide, is available and if a post-deposition anneal at an elevated temperature is employed.

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14. ABSTRACT

This thesis focuses on two aspects of oxide-based thin-film transistors (TFTs), contact resistance and instability assessment. First, determination of the contact resistance of indium tin oxide (ITO) on two wide-band gap semiconductors, zinc oxide (ZnO) and indium gallium oxide (IGO), is attempted and the effects of contact resistance on device performance is investigated. Both transistor and transfer length method (TLM) structures are used in the study and three material systems are employed: ZnO on SiO2, ZnO on aluminum titanium oxide (ATO), and IGO on SiO2. It is found that the measured resistance is not dominated by contact resistance effects. It is concluded that the device dimensions used in this study (i.e., gate lengths of 50 to 200 μm) are too large to yield an accurate estimate of the contact resistance, since it is so small. Second, a methodology for assessing the stability of oxide-based TFTs is developed and implemented. This methodology involves constant voltage stressing over a maximum duration of 105 s (i.e., ~ 28 hours) and periodic evaluation of drain current-drain voltage and drain current-gate voltage characteristics during the stability test. This stability assessment strategy is first applied to three semiconducting materials: ZnO, zinc indium oxide (ZIO), and IGO, using thermal silicon oxide as the gate dielectric. Similar trends are observed for these device types. Relatively stable devices are obtained after post-deposition annealing at a temperature of ~ 600 ?C for ZnO and IGO TFTs, and ~ 400 ?C for ZIO TFTs. The presence of instability in these devices, which is more pronounced at a lower annealing temperature, results in a positive shift in the turn-on voltage and clockwise hysteresis in the drain current-gate voltage transfer curve. Such an instability is attributed to electron trapping near the channel/insulator interface. The stability a ZnO TFT fabricated using a spin-coat synthesized aluminum phosphate (AlPO) as the gate dielectric is also investigated. The ZnO/AlPO TFT showed distinctively different stability trends. This device is observed to be very unstable with a negative shift in the turn-on voltage and counter-clockwise hysteresis in the drain current-gate voltage transfer curve. The mechanism for this instability is ascribed to insulator ion drift. It is shown that stable TFTs can be fabricated with oxide-based channel layers if a high quality insulator, such as thermal silicon dioxide, is available and if a post-deposition anneal at an elevated temperature is employed.

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CONTACT RESISTANCE AND STABILITY ANALYSIS OF OXIDE-BASED THIN FILM TRANSISTORS

1. INTRODUCTION

Transparent electronics is a new field of research which began with the introduction of the first transparent thin-film transistor (TTFT) in 2003 [1,2]. To date, the majority of reported TTFT's employ a zinc oxide (ZnO) channel layer [3,4,5,6,7]. ZnO is just one of many materials that can be categorized as a heavy metal cation (HMC) with an $(n-1)d^{10}ns^{0}(n \geq 4)$ electronic configuration, where "n" refers to the row of the periodic table [8]. Current research focuses on material development, exploring both HMC's and amorphous multicomponent heavy metal cation (a-MHMC) oxides for transparent channel material applications. Materials investigated to date for transparent channel material applications include tin oxide [9], amorphous indium gallium zinc oxide [10], zinc tin oxide (ZTO) [11], zinc indium oxide (ZIO) [12], and indium gallium oxide (IGO) [13].

To date, very little effort has been invested into assessing the contact resistance and device stability of oxide-based transistors. The goal of this thesis is two-fold. First, this thesis investigates the effects of contact resistance on ZnO, ZIO, and IGO based thin-film transistors deposited on both glass and silicon substrates. Secondly, this thesis introduces and applies a standardized process for assessing the stability of oxide-based thin-film transistors (TFTs).

The chapters constituting this thesis are as follows. Chapter 2 provides technical background related to thin-film transistor operation, electrical characterization figures of merit for TFTs, and material properties of ZnO, ZIO, and IGO. Chapter 3 describes procedures used for device fabrication, as well as characterization tools and techniques for measuring contact resistance. Chapter 4 presents an in-depth electrical characterization study of TFTs fabricated with ZnO, ZIO, and IGO channel layers on glass and silicon substrates, focusing on the effects of contact resistance. Chapter 5 develops and utilizes a methodology standard for assessing the stability of oxide-based thin-film transistors. Chapter 6 contains conclusions and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

This chapter explores previously reported work and fundamental concepts crucial to the understanding of TFTs. A brief discourse on multicomponent heavy metal cation (MHMC) oxides is included. The properties of ZnO, ZIO, and IGO are discussed in preparation for the results presented in Chapters 4 and 5. TFT operation and electrical characterization figures-of-merit are presented. Figures-of-merit for contact resistance and stability assessment are also addressed.

2.1 Thin-film transistors

TFTs constitute a class of field-effect transistors in which a thin-film layer is deposited to create the gate dielectric, the active channel layer, and the source and drain contacts. The following subsections delve into TFT layout, operation, and figures-of-merit for electrical characterization.

2.1.1 Thin-film transistor structures and basic operation

There are four basic layouts for a TFT, as illustrated in Fig. 2.1: (a) staggered bottom-gate, (b) co-planar bottom-gate, (c) staggered top-gate, and (d) co-planar top-gate. The terms staggered and co-planar refer to the placement of the electrodes. Staggered structures are laid out such that the source/drain contacts are placed on one side of the semiconductor/insulator interface, while the gate electrode is placed on the opposing side of the interface. In the co-planar layout, gate and source/drain contacts are placed on the same side of the semiconductor/oxide interface. Each of the four basic layouts has advantages and disadvantages in regard to processing and integration [14]. As a consequence of processing considerations, a staggered bottom-gate structure is employed in this research.

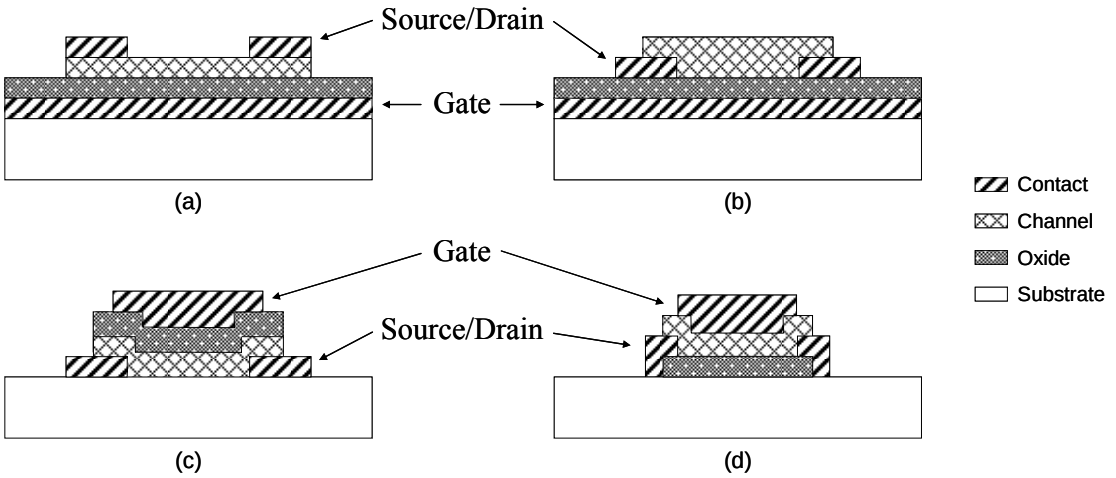

Figure 2.1: Four basic thin-film transistor structures: (a) staggered bottom-gate, (b) co-planar bottom-gate, (c) staggered top-gate, and (d) co-planar top-gate.

TFTs may be classified as enhancement-mode and depletion-mode. A TFT is identified as a depletion-mode device if application of a gate bias is required to turn the device "off", i.e., to stop current flow in the channel. If a gate voltage is necessary to turn the device "on", i.e., to form a channel and induce current flow, it is considered an enhancement-mode device.

Figure 2.2 shows energy band diagrams for an n-type, accumulation-mode TFT under various bias conditions. When no gate bias is applied, the energy bands are assumed to be at flat-band, an ideal case situation, as indicated by Fig. 2.2a. When a negative voltage is applied to the gate, delocalized electrons in the channel layer are repelled from the semiconductor/gate interface. This process creates a region of positive charge referred to as a depletion region (i.e., depleted of negative charge). The collection of positive charge near the interface creates a positive (upwards) curvature in the conduction and valence bands, as shown by Fig. 2.2b. When a positive voltage is applied to the gate, delocalized electrons create an accumulation region due to the attraction of the electrons to the semiconductor/insulator interface. This accumulation of negative charge causes the energy bands to curve negatively (downwards), as illustrated in Fig. 2.2c.

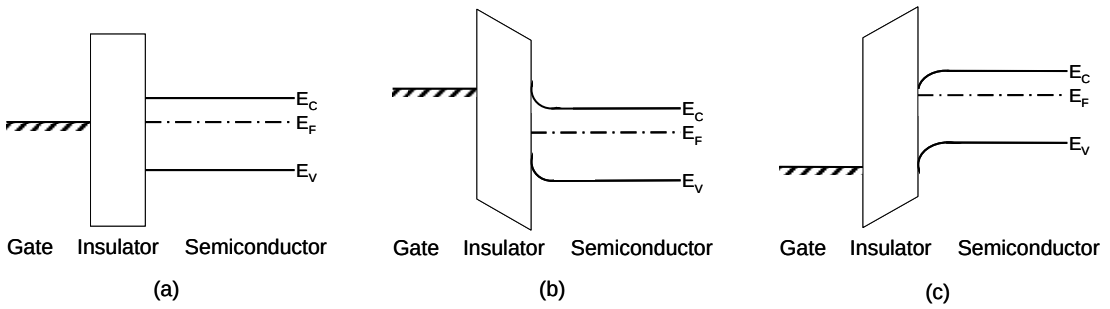

Figure 2.2: Energy band diagrams for a typical n-type, accumulation-mode TFT. (a) Under ideal conditions, flat-band, $V_G = 0$ V. (b) Depletion of carriers results in an upward band bending with applied negative gate bias, $V_G < 0$ V. (c) Accumulation of carriers creates a downward band bending with applied positive gate bias, $V_G > 0$ V.

The TFT is said to be "on" when current is allowed to flow thorough the channel layer from the source to the drain. This occurs when the applied gate voltage is larger than the voltage needed to turn on the device, $V_{GS} \geq V_{ON}$, where V_{GS} is the gate-to-source voltage, and V_{ON} is the turn-on voltage, which is defined as the gate voltage at which the drain current begins to increase [6]. Current conduction is the result of the extraction of accumulated electrons from the channel and has the following relationship,

$$I_{DS} = \mu C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}\right] \ (0 \leq V_{DS} \leq V_{DS,sat} \text{ and } V_{GS} \geq V_{ON}), \qquad (2.1)$$

where, V_{DS} is the drain-to-source voltage, C_{OX} is the oxide capacitance, μ is the electron channel mobility, W and L are the width and length dimensions of the channel, respectively, and $V_{DS,sat}$ is the pinch-off voltage. Channel pinch-off is defined as the voltage at which the region of the channel nearest the drain is depleted of electrons, and the drain current is independent of V_{DS}. Pinch-off occurs when $V_{DS} = V_{DS,sat}$, where $V_{DS,sat} = V_{GS} - V_{ON}$, in which case Eq. 2.1 becomes,

$$I_{DS} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{ON})^2, \ (V_{DS} \geq V_{DS,sat} \text{ and } V_{GS} \geq V_{ON}). \qquad (2.2)$$

For drain-to-source voltages exceeding the pinch-off condition, the TFT operates in the saturation regime. Equations 2.1 and 2.2 constitute the "square-law" theory, which is also applicable to the

operation of a metal-oxide-semiconductor field-effect transistor (MOSFET). Figure 2.3 illustrates typical I_D-V_{DS} characteristics.

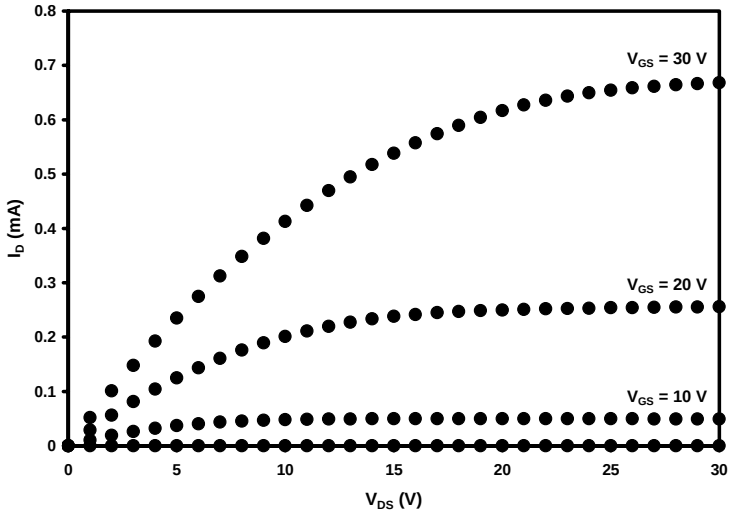

Figure 2.3: I_D-V_{DS} characteristics for a TFT composed of a IGO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm. 0 V ≤ V_{DS} ≤ 30 V in 1 V steps and 0 V ≤ V_{GS} ≤ 30 V in 5 V steps. I_D increases with increasing V_{GS}.

2.1.2 Figures of merit

DC electrical characterization of TFTs and TTFTs involves collection of data which is used to assess device performance. There are three main figures-of-merit used to characterize a device: turn-on voltage, drain current on-to-off ratio, and channel mobility.

The turn-on voltage is defined as the gate voltage at which the drain current, I_D, increases above the gate leakage current, I_G, on a log(I_D)-V_{GS} plot (for small values of V_{DS}) [6]. Drain current on-to-off ratio, $I_{ON\text{-}OFF}$, is the ratio of the maximum to minimum drain current at high V_{DS} to ensure that the device is operating in the saturation regime. V_{ON} and $I_{ON\text{-}OFF}$ are shown in Fig. 2.4. The on-to-off current ratio is on the order of 10^6, the turn-on voltage is 2 V, and the gate leakage current is approximately 0.1 nA.

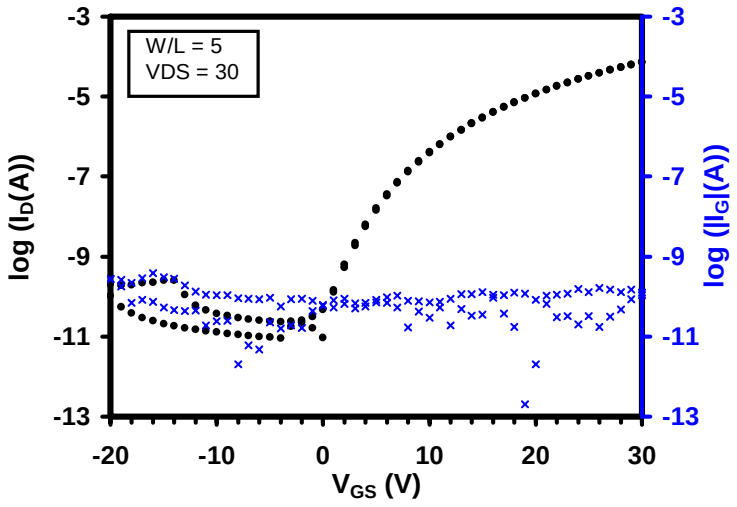

Figure 2.4: Typical log(I_D)-V_{GS} plot illustrating the drain current, I_D, gate leakage current, I_G, turn-on voltage, V_{ON}, and the drain current on-to-off ratio, $I_{ON\text{-}OFF}$. $I_{ON\text{-}OFF}$ is 10^6 and V_{ON} is 2 V. The DUT is a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm.

Channel mobility is a critical figure-of-merit for characterizing a TFT. Mobility determines the performance of a thin-film transistor in terms of current drive and frequency response. Channel mobility for a TFT is discussed in detail by Hoffman [6]. There are two types of mobility of relevance to this thesis: incremental mobility, μ_{inc}, and average mobility, μ_{ave}. Average mobility is the average of all the carriers present in the channel and is directly proportional to the channel conductance, G_{CH}, by [6]

$$\mu_{ave}(V_{GS}) = \frac{G_{CH}(V_{GS})}{\frac{W}{L} C_{ins}(V_{GS} - V_{ON})}, \tag{2.3}$$

where

$$G_{CH}(V_{GS}) = \lim_{V_{DS}\to 0} \left(\frac{\partial I_D}{\partial V_{DS}} \right)\Bigg|_{V_{GS}}. \tag{2.4}$$

Incremental mobility is the mobility of the carriers added to the channel as the gate voltage is incrementally increased in magnitude and is proportional to the differential channel conductance as follows, [6]

$$\mu_{inc}(V_{GS}) = \frac{G'_{CH}(V_{GS})}{\frac{W}{L}C_{ins}}, \tag{2.5}$$

where

$$G'_{CH}(V_{GS}) = \frac{dG_{CH}}{dV_{GS}}. \tag{2.6}$$

Equations 2.3 and 2.5 for μ_{ave} and μ_{inc} are nearly identical to the corresponding equations for effective mobility (μ_{eff}) and field-effect mobility (μ_{FE}), respectively, the difference being that the average mobility is a function of V_{ON} rather than V_T as used for an ideal FET and that the incremental mobility is defined in terms of the differential channel conductance rather than the transconductace [15]. Figure 2.5 shows typical μ_{ave} and μ_{inc} values as a function of gate bias; the maximum incremental mobility is 5.7 cm^2/V-s and the maximum average mobility is approximately 2 cm^2/V-s.

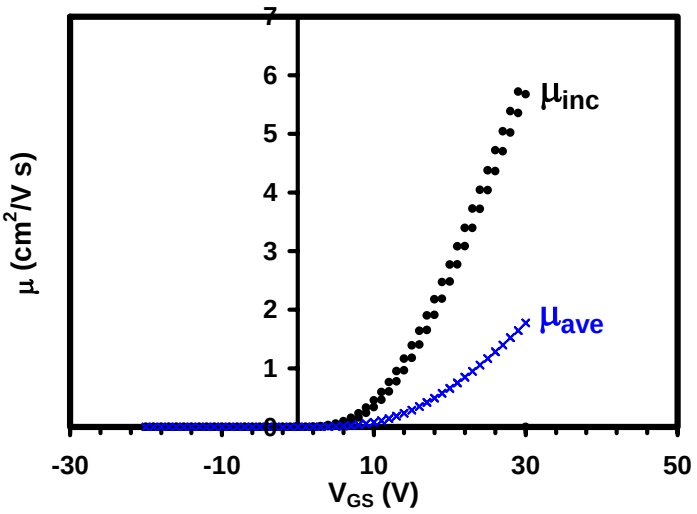

Figure 2.5: Extracted average and incremental (μ_{ave} and μ_{inc}) mobility as a function of gate bias for a ZnO TFT fabricated on thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm. The maximum mobilities are μ_{ave} = 5.7 cm^2/V-s and μ_{inc} 2 cm^2/V-s.

2.2 Transparent conducting oxides

Transparent conducting oxides (TCOs) are wide-bandgap semiconductors. They are extensively used in TTFTs, solar cells, active-matrix displays, and also for conductive and optical coatings. The most widely used TCO is indium tin oxide (ITO). In 1996, Hosono *et al*. proposed that a new class of TCOs could be created from a combination of multicomponent oxides composed of heavy metal cations (HMCs) with an $(n-1)d^{10}ns^{0}(n \geq 4)$ electronic configuration. Many new TCOs have been developed based on this proposition. Amorphous semiconducting materials such as $AgSbO_3$, Cd_2PbO_4, Cd_2GeO_4 [8], ZTO [11], ZIO [12], IGO [13] have been developed. Single cation oxides such as polycrystalline ZnO [1, 2, 3, 4, 7] and SnO_2 [9], as well as the single-crystalline, quaternary compound IGZO [5] have also been demonstrated as channel materials. ITO, ZnO, ZIO, and IGO are discussed in more detail in subsequent subsections, as these materials are used in the focus of this research and are summarized in Table 2.1.

2.2.1 Indium tin oxide

Indium tin oxide (ITO), or tin-doped indium oxide, is a TCO that is used for many applications ranging from conductive and optical coatings, solar cells, flat-panel displays, and gas sensors. For TFT and TTFT applications, ITO is routinely employed as the gate, source, and drain electrode [1, 2, 5, 6, 7, 9, 10, 11, 12, 13]. The widely accepted standard composition of ITO is 10% tin by weight. Tahar *et al.* conclude that the material properties of ITO vary greatly depending on deposition parameters: method of deposition, oxygen partial pressure, source material, film thickness, as well as substrate temperature [16]. Hall mobilities for ITO deposited via evaporation have been reported in the range of 16-70 cm^2/V-s and 16-41 cm^2/V-s for direct current (dc) and rf magnetron sputtering, respectively. In the case of chemical vapor deposition (CVD), carrier mobilities range from 5 cm^2/V-s to 70 cm^2/V-s depending upon the gaseous reactants used in depositing the ITO film.

2.2.2 Zinc oxide

ZnO is the most extensively studied wide-bandgap material for both TFT and TTFT applications. The first TTFT was announced by Masuda *et al.* in 2003. This TTFT is fabricated with a ZnO channel layer deposited via pulsed laser deposition (PLD) at 450° C [1]. Devices use a double layer gate dielectric in order to minimize gate leakage. The dielectric stack is comprised of SiO_2 and SiN_X. Indium zinc oxide is employed for the source and drain electrodes. Devices fabricated by Masuda *et al.* resulted in a maximum mobility at 0.97 cm^2/V-s, a drain current on-to-off ratio $>10^5$, and a threshold voltage, V_T, of -1 V.

Also in 2003, Hoffman *et al.* demonstrated the first fully transparent ZnO TTFT fabricated on a glass substrate [2]. The ZnO is deposited via ion beam sputtering and rapid thermal annealed from 600-800 °C. The gate dielectric is aluminum titanium oxide (ATO), a superlattice comprised of alternating layers of Al_2O_3 and TiO_2. The source and drain contacts are ITO deposited via ion beam sputtering. The highest mobility reported is 2.5 cm^2/V-s with a drain current on-to-off ratio $>10^5$, and V_T between 10-20 V.

Carcia *et al.* revealed a ZnO channel TFT on a silicon substrate in 2003 [3]. The channel layer is deposited via radio frequency (RF) magnetron sputtering near room temperature on thermal silicon dioxide, which acts as the gate insulator. The source and drain contacts are Ti/Au. Such devices showed mobilities of 2 cm^2/V-s and drain current on-to-off ratios of $>10^6$. V_T is reported to be ~ 0 V.

Nishi *et al*. created TFTs using a $CaHfO_X$ buffer layer between an a-SiN gate dielectric and the ZnO channel layer [4]. The channel layer is deposited via PLD at 300 °C with aluminum for the source and drain electrodes. Nishi *et al.* show that the buffer layer increased the mobility by as much as 2 cm^2/V-s to 7 cm^2/V-s. Devices also showed drain current on-to-off ratio of 10^6. The devices fabricated in this study are competitive with commercial a-Si TFTs used in active-matrix displays.

Similar to Carcia *et al.,* Fortunato *et al.* demonstrated a ZnO channel TFT via RF magnetron sputtering processed at room temperature [7]. ATO is used as the gate dielectric while gallium-doped zinc oxide is deposited as the source and drain electrodes. Devices operated with a channel mobility of 27 cm^2/V-s, a drain current on-to-off of ~ 10^5, and a V_T of 19 V.

2.2.3 Zinc indium oxide

A MHMC oxide that has been developed at Oregon State University is ZIO. In 2005, Dehuff *et al.* demonstrated a high-mobility TTFT with ZIO [12]. The ZIO TTFT uses a glass substrate with ATO acting as the gate insulator and ITO as the gate and source/drain contacts. The ZIO is deposited via RF magnetron sputtering with no intentional heating. Both enhancement-mode and depletion-mode devices are fabricated based on anneal temperatures of 300 and 600 °C, respectively. Depletion-mode TFTs exhibit mobilites in the range of ~ 45-55 cm^2/V-s, drain current on-to-off ratios of ~ 10^6, threshold voltages ~ -20 to -10 V, and a turn on voltage ~ 3 V less than the V_T. Enhancement-mode devices, on the other hand, perform with mobilites in the range of 10-30 cm^2/V-s, V_T ~ 0-10 V, and V_{ON} ~ 1-2 V less than V_T. Room temperature enhancement-mode ZIO TTFTs are also fabricated. Such devices exhibit a peak channel mobility of 8 cm^2/V-s and a drain current on-to-off-ratio of 10^4.

2.2.4 Indium gallium oxide

Indium gallium oxide is an amorphous MHMC oxide compound that has been demonstrated as a TCO. Chiang *et al.* demonstrated a-IGO TTFTs [13]. The IGO channel layer is RF sputtered from a ceramic target with no intentional substrate heating. The stack is then subsequently furnace annealed at 600 °C resulting in a peak channel mobility of ~ 27 cm^2/V-s, a drain current on-to-off ratio >10^6, and V_{ON} = -14 V. Chiang *et al.* also fabricate a-IGO devices at a low temperature of 200 °C. Such devices exhibit a mobility of ~ 19 cm^2/V-s and a V_{ON} of 2 V.

Channel Material	Process Temp. (° C)	Deposition Method	Source/Drain Electrodes	Peak Mobility (cm^2/V-s)	I_{On-Off}	Threshold Voltage (V)	Ref
ZnO	450	PLD[2]	IZO	0.97	$>10^5$	-1	[1]
ZnO	600-800	IBS[3]	ITO	2.5	$\sim 10^7$	~ 10-20	[2]
ZnO	R.T.[1]	RFMS[4]	Ti/Au	2	$>10^6$	~0	[3]
ZnO	300	PLD[2]	Al	7	10^6		[4]
ZnO	R.T.[1]	RFMS[4]	GZO	27	10^5	19	[7]
ZIO	600	RFMS[4]	ITO	~ 45-55	10^6	~ -20-(-10)	[12]
IGO	600	RFMS[4]	ITO	~ 27	$>10^6$	-14	[13]

[1] room temperature
[2] pulsed laser deposition
[3] ion beam sputtering
[4] radio frequency magnetron sputtering

Table 2.1: Summary of wide-bandgap semiconductors utilized as the channel layer in TFTs and TTFTs. Deposition methodology, process temperature, as well as electrical characterization figure-of-merits are listed.

2.3 Contact resistance

Contact resistance can affect device performance and therefore is an important parameter to examine. The measured resistance in a transistor is the resistance seen between the source and the drain electrodes. This resistance includes the parasitic source resistance, R_S, the channel resistance, R_{CH}, and also the parasitic drain resistance, R_D. The parasitic resistances are often referred to as the contact resistance. The voltage applied across the source and drain of a transistor, terminals S and D in Fig. 2.6, may differ from the voltage dropped across S' and D' if parasitic resistances are large. When R_S and R_D are large, a higher applied bias is needed across the source and drain to inject carriers into the device, resulting in lower reported mobilities.

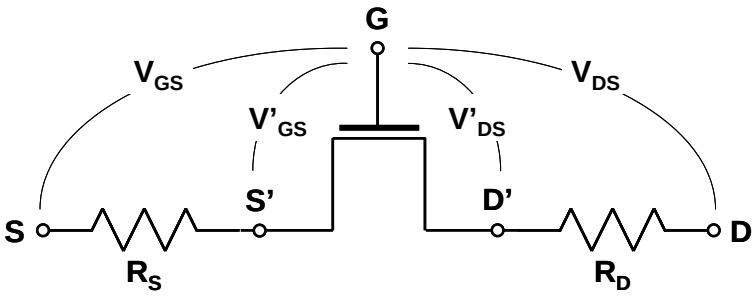

Figure 2.6: Schematic showing an intrinsic transistor with a lumped parameter representation of the source and drain resistances.

2.3.1 Previous work

Since contact resistance can affect device performance, there have been various reports on the effect of contact resistance for hydrogenated amorphous silicon (a-Si:H) and organic TFTs which are summarized in this section. Luan and Neudeck reported that the parasitic resistances are determined by current crowding under the source/drain regions, as shown by Fig. 2.7 [17].

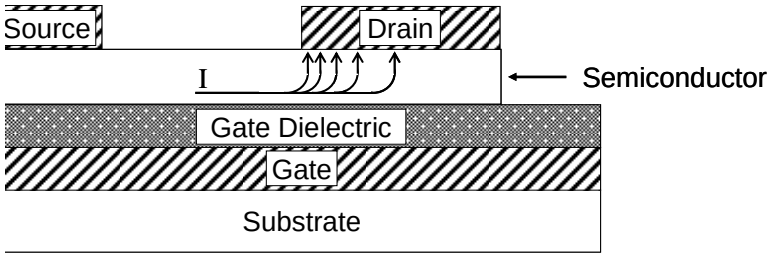

Figure 2.7: TFT cross-section showing current crowding in the drain/gate overlap. Since current flows in a path of least resistance, more current will flow from the channel into the region of the drain contact closest to the source electrode. Notice that current does not necessarily flow through the entire overlap region.

During their investigation of device performance as a function of the thickness of a-Si:H TFTs, Martin *et al.* confirmed the findings of Luan and Neudeck by reporting that the entire source/gate and drain/gate contact overlap does not affect electrical performance as current does not flow over the entire overlapped region [18].

For TFTs fabricated with an organic channel layer, Blanchet *et al.* found a correlation between contact resistance and the dielectric material used as the gate insulator [19]. This observed correlation

may result from a chemical interaction at interface layers (i.e., dielectric/electrode and dielectric/semiconductor). Klauk *et al.* demonstrated for large channel lengths, the channel resistance is large and dominates, whereas at small channel lengths, the channel resistance is small in comparison to the parasitic resistance, and thus the contact resistance dominates [20].

Very little work has been published on the effect of contact resistance in TFTs fabricated with wide-bandgap semiconductors. In a recent publication, Jackson *et al.* reported that the contact resistance of ITO has a negligible effect on the device performance of flexible transistors employing ZTO as the channel layer [21].

2.3.2 Techniques for determining contact resistance

There are many experimental techniques for determining contact resistance. Contact resistance can be determined by using a variety of structures such as a two-terminal structure, a multiple-terminal structure including the transfer line method (TLM) test structure, Kelvin test structures, pn-junctions, Schottky barrier diodes, solar cells, bipolar junction transistors, and MOSFETs [15]. For a MOSFET test structure, physical device parameters such as channel width, channel length, and source/gate and drain/gate overlap distance can be varied to observe how these parameters effects contact resistance. Various analytical techniques have been proposed for extracting contact resistance from a MOSFET test structure. Terada *et al.* extracts the contact resistance, R_{SD}, from the measured resistance, R_M, versus channel length, L, plot using the following analytical expression, [15]

$$R_M = \frac{V_{DS}}{I_D} = \frac{(L - \Delta L)}{(W - \Delta W)\mu_{eff} C_{OX}(V_{GS} - V_{ON})} + R_{SD}, \tag{2.8}$$

where $\Delta L = L - L_{eff}$ as illustrated by Fig 2.8; ΔW is the analogy of ΔL, in which $\Delta W = W - W_{eff}$.

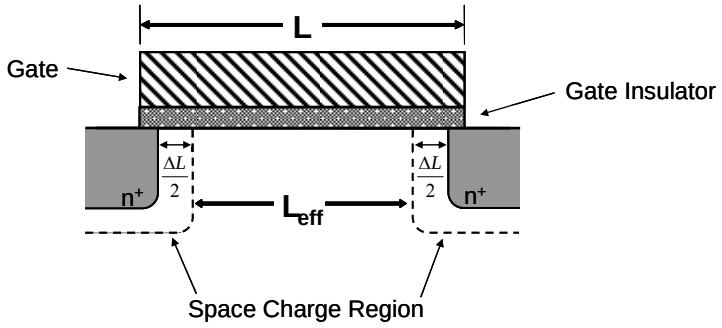

Figure 2.8: Device cross-section for a MOSFET showing the drawn gate length, L, effective gate length, L_{eff}, and ΔL. $L_{eff} = L - \Delta L$

Luan and Neudeck use an approach similar to that of Terada *et al.* for determining the parasitic source/drain resistance in an a-Si:H TFT [17]. Since their experiment used varying channel widths, Luan and Neudeck normalized R_M and R_{SD} by the width. Thus, $R_{SD} \cdot W$ is extracted from a $R_M \cdot W$ versus L plot. Suciu and Johnston suggest a different approach in which the contact resistance is extracted from a parameter E [15]. The parameter E is defined as

$$E = R_M\left(V_{GS} - V_T\right) = \frac{\left(L - \Delta L\right)}{W_{eff}\,\mu_{eff}\,C_{OX}} + R_{SD}\left(V_{GS} - V_T\right), \tag{2.9}$$

where $W_{eff} = W - \Delta W$ and V_T is the threshold voltage,i.e., the voltage at which the channel in a MOSFET is formed and begins to conduct current. Similar to the Suciu *et al.* method, de la Moneda extracts R_{SD} from the following equation, [15]

$$R_M = \frac{L - \Delta L}{W_{eff}\,\mu_{eff}\,C_{OX}\left(V_{GS} - V_T\right)} + \frac{\theta\left(L - \Delta L\right)}{W_{eff}\,\mu_0 C_{OX}} + R_{SD}\,. \tag{2.10}$$

A variation of the de la Moneda technique involves the extraction of R_{SD} via [15]

$$I_D = \frac{W_{eff}\,\mu_0 C_{OX}}{L_{eff}} \frac{\left(V_{GS} - V_T\right)\left(V_{DS} - I_D R_{SD}\right)}{1 + \theta\left(V_{GS} - V_T\right)}. \tag{2.11}$$

ITO is employed in this research as an injecting contact for the source and drain electrodes. The methods proposed by Terada *et al.*, Luan and Neudeck, and TLM test structures are used in this thesis to determine if the contact resistance of ITO on wide-band gap semiconductors such as ZnO, ZIO, and IGO effects device performance. The physical device parameters channel width, channel

length, and source/channel and drain/channel overlap distance for a bottom-gate TFT are varied in this experiment. Chapter 4 discusses the contact resistance estimation methodology used in detail, such as device layout, testing techniques, as well as data interpretation.

2.4 Stability assessment

Reliability is a crucial factor if a material is to be manufactured on a large scale for future applications such as circuits. Significant effort has been invested into developing new materials for TFT applications while assessing instabilities and their origin in new TCOs have received very little attention.

Instabilities have been explored for MOSFETs, a-Si:H TFTs and also organic TFTs (OTFTs). Before a method for assessing if a material system and/or a device can be determined to be stable or unstable, stability criteria must be defined. As summarized by Wang, degradation in a MOSFET is characterized by a shift in V_T, change in the transconductance of the device, which is related to the change in mobility, and a decrease in the subthreshold slope [22]. Transconductance is a MOSFET parameter that characterizes channel conductivity.

Gleskova and Wagner found that when applying a constant voltage to the gate of an a-Si:H TFT fabricated on a polyimide foil substrate, bias stressing causes an increase in both V_T and the subthreshold slope, a decrease in the mobility, and no change in the drain current on-to-off ratio [23]. The changes observed in the threshold voltage, subthreshold slope, and mobility are more pronounced with an increase in stress time and/or gate bias. Gleskova and Wagner also reported that the changes observed in the subthreshold slope and mobility are reversible after a period of rest (i.e., no applied voltage).

In 1997, Brown *et al.* published an in-depth report on OTFT reliability. Brown et al. demonstrated that while a shift in V_T occurs, the source-drain current curve as a function of gate bias does not change in shape after bias stressing but is shifted along the gate voltage axis [24]. It is also found that after a prolonged amount of resting, the devices recovered to their original characteristics.

The term instability has been used synonymously with the presence of hysteresis and threshold voltage shift. However, there are other manifestations of instability, such as changes in the drain current magnitude, the mobility, and the subthreshold slope. Hysteresis refers to an electrical characteristic, usually I_D for the case of FETs, which does not retrace itself when subjected to a continuous cyclic voltage ramps in forward and reverse directions. An example of transfer curve hysteresis is depicted in Fig. 2.9.

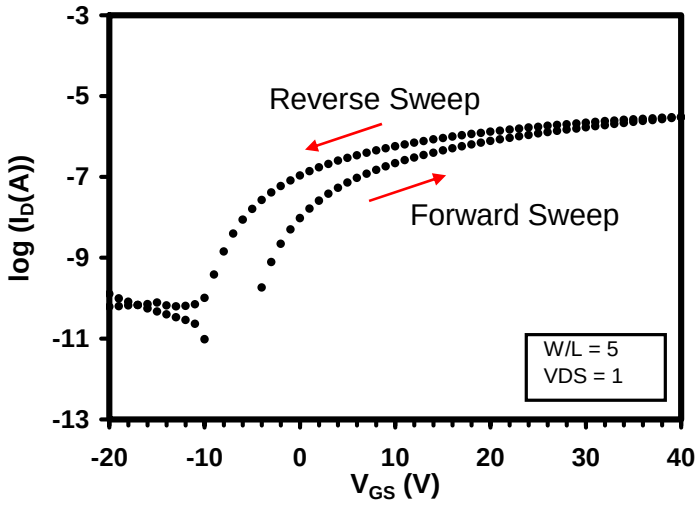

Figure 2.9: A $\log(I_D)$-V_{GS} transfer curve showing hysteresis for a ZnO channel (~ 50 nm) TFT fabricated on gate dielectric material of aluminum oxide phosphate. For the forward sweep, V_{ON} = -4 V, the reverse sweep gives V_{ON} = -10 V. The sweep rate is ~ 1V/s

The work reported in this thesis applies the principles and techniques published for instability analysis of MOSFETs, a-Si:H TFTs, and OTFTs to the assessment of instabilities in TFTs fabricated with wide-bandgap semiconductors. The criteria developed in this thesis for characterizing instabilities are as follows: shift in V_{ON}, a change I_D, a change in the peak channel mobility, and also the presence of hysteresis. Chapter 5 of this thesis discusses in detail a methodology proposed for assessing instabilities in TFT devices processed with ZnO, ZIO, and IGO channel layers.

2.5 Conclusions

In this chapter, basic TFT operation and figures-of-merit are presented. A brief introduction into transparent conducting oxides including TCOs composed of multi-component heavy metal cations is provided. Previous work related to ITO, ZnO, ZIO, and IGO is reviewed. The importance of contact resistance on device performance is discussed. Finally, previous work related to instabilities in MOS devices, amorphous silicon TFTs, and organic TFTs is considered.

3. EXPERIMENTAL TECHNIQUES

This chapter describes deposition methods and techniques utilized in the research leading to this thesis. Thin-film deposition processing tools and methodology are discussed. Additionally, electrical characterization techniques for determining contact resistance and assessing device stability are explored.

3.1 Thin-film processing

This section presents information on the processing methods and tools used in the fabrication of TFTs and TTFTs utilized in this work. Physical vapor deposition (PVD), patterning, and post-deposition anneal processes are discussed.

3.1.1 Physical vapor deposition

PVD is a thin-film deposition method whereby materials are physically transferred under vacuum conditions from a solid source, generally called a target, to the surface of a substrate. This section discusses thermal evaporation, RF magnetron sputtering, and ion beam sputtering, which are PVD processes used in this work.

3.1.1.1 Thermal evaporation

Thermal evaporation is a thin-film deposition technique typically used to deposit metals with low melting temperatures. Evaporation is the process in which a material is heated and vaporizes. The vaporized material collects and cools on the surface of a substrate to create a thin-film of the source material. Thermal evaporation is performed under high vacuum, typically $\leq 5 \times 10^{-6}$ Torr. The evaporation process begins with a high current (~ 20 A for Al) sent through a filament or “boat” that holds the material to be evaporated. The filament is made of a refractory metal, i.e., a metal with an

high melting point, such as tungsten. Current flows through the filament causing the filament and source material to heat up due to resistive heating, resulting in the vaporization of the source material. Aluminum is thermally evaporated as the source and drain electrodes for TFT devices fabricated for investigating channel material stability.

3.1.1.2 RF magnetron sputtering

Sputtering is a deposition method where atoms from a target are transferred and redeposited onto the surface of a substrate. Atoms from the negatively biased target are knocked loose by positively charged ions, created within a plasma and are deposited on a nearby substrate. A plasma, also known as a glow discharge, is an ionized gas comprised of of electrons and ions. The plasma provides a source of positively charge ions used to bombard the target during the sputtering process. The term magnetron sputtering refers to a sputtering process in which the plasma is shaped by a magnetic field. RF indicates that a power supply with an alternating voltage, typically operating at a frequency of 13.56 MHz, is employed to create the plasma.

RF magnetron sputtering is performed under vacuum, typically between 1 mTorr and 50 mTorr. This range of pressure controls the quality of the deposited film and the rate at which it is deposited. This PVD process can be used to deposit both insulating and conducting materials. The main drawbacks of RF sputtering are cost and deposition rate. The cost of an RF power supply is greater than that of a DC supply. The deposition rate with an RF power supply is lower in comparison to a DC power supply, as a DC source supplies continuous voltage, whereas a RF source has alternating voltage. RF magnetron sputtering is used to deposit channel layers for TFTs fabricated for both contact resistance study and instability assessment.

3.1.1.3 Ion beam sputtering

Ion beam sputtering is a form of sputtering which uses a DC power supply rather than a RF supply to generate a plasma. While conventional DC sputtering can be used to sputter conductive materials, it cannot be used to deposit insulating materials since it causes a charge build-up on the

surface of the target; the result is the extinguishing of the plasma. Ion beam sputtering, however, can be used to deposit insulating materials since the plasma is created in a separate chamber from the target and the ions are accelerated towards the target passing by a neutralizing filament. The neutralizing filament is used to eliminate the positive charge associated with the ions, preventing a charge build-up at surface of the insulating target. Ion beam sputtering is used to deposit conductive ITO for the source and drain contacts for TFTs fabricated for exploring the effect of contact resistance.

3.1.2 Thin-film patterning

Thin-film patterning involves the creation of defined geometries in a thin-film. A pattern can be defined in many ways, such as through the use of shadow masks, photolithography, etching, and lift-off; these techniques are presented in the following sections.

3.1.2.1 Shadow mask

A shadow mask is a thin sheet of material with openings used to define geometries onto a surface during thin-film processing. The mask is placed directly on top of the substrate, allowing material to be deposited onto the exposed substrate surfaces, as shown by Fig. 3.1. Aluminum shadow masks are used to define channel and source and drain geometries for devices used to investigate channel material stability. Device dimensions using shadow masks are typically large in comparison to photolithography methods.

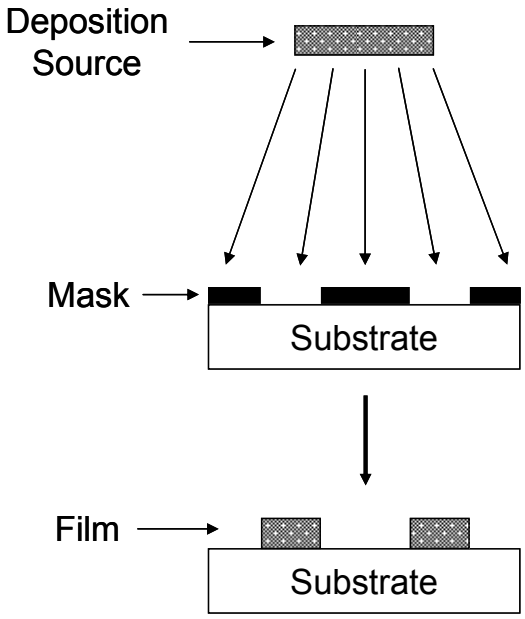

Figure 3.1: Cross-section showing the patterning of a film via a shadow mask.

3.1.2.2 Photolithography

Photolithography is a common process of pattern transfer used in the semiconductor industry. An image on a mask is transferred to a material called photoresist with the use of ultraviolet (UV) light. Photoresist is an organic polymer whose chemical properties change, i.e., the solubility of the photoresist, when it is exposed to UV light.

There are two types of photoresist: positive and negative resist. Positive resist is insoluble and becomes soluble after exposure from a UV light source due to the weakening of chemical bonds. An exact copy of the image on the mask is transferred directly to the resist. Negative resist is initially soluble and becomes insoluble after exposure from a UV light source due to the strengthening of chemical bonds. An inverted copy of the image on the mask is transferred to the resist. Figure 3.2 illustrates the pattern transfer for both positive and negative resist.

Photolithography begins by spin coating a substrate with photoresist. A bake step, known as a soft bake, follows. The soft bake improves adhesion of the resist to the surface of the substrate and drives out excess solvent from the photoresist. The image from a mask is then transferred to the resist

by exposure and development. Exposure is the process where the resist is illuminated under a UV light source. Development is the process where the soluble resist is removed. After exposure, the sample is submersed in a liquid solvent called developer which removes the soluble resist, leaving behind the desired pattern. Minimum device dimensions using photolithography are much smaller than devices fabricated with shadow masks.

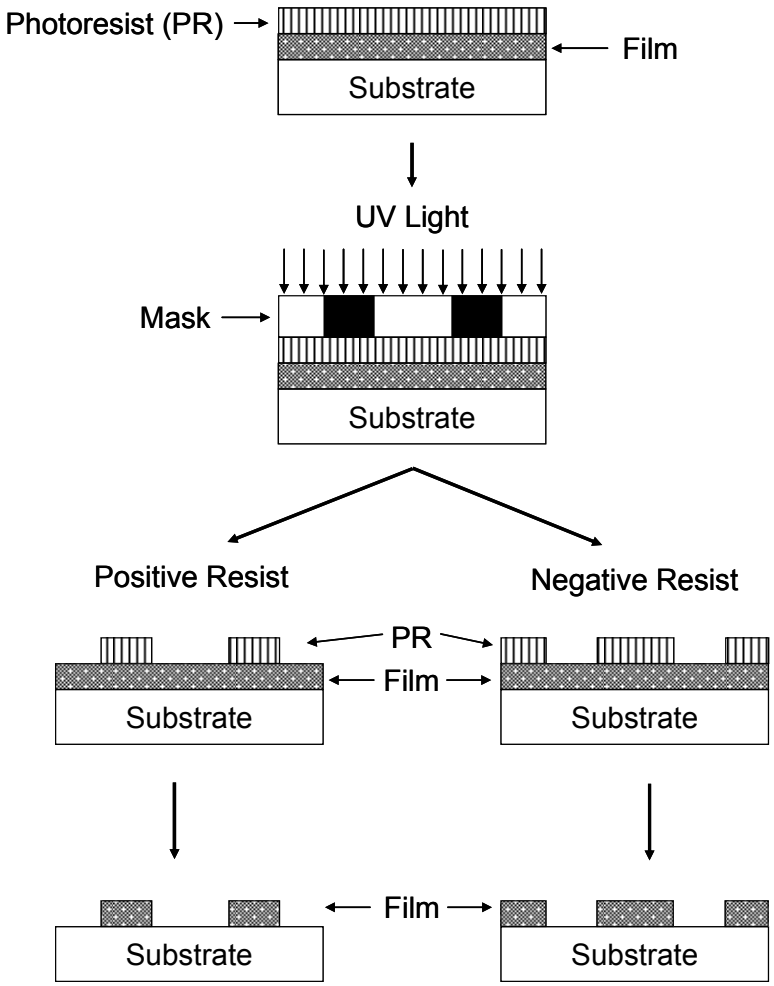

Figure 3.2: Cross-section showing the patterning of a film using both positive and negative photoresist.

3.1.2.3 Etching process

Etching is the process where a material is removed from a substrate; it is a subtractive process. There are two important etch parameters: etch selectivity and etch profile. Etch selectivity refers to a selected material being removed at a different rate than another material present on the surface of the substrate, e.g., the etch rate needs to be higher for a film than for photoresist. Etch profile refers to the topology of the film surface after etching. An etch profile is either isotropic or anisotropic. An isotropic etch removes material in all directions at an equal rate. An anisotropic etch removes material in a particular direction, usually associated with a crystal or surface direction.

While there are three types of etching: wet chemical etching, dry or physical etching, and reactive ion etching, a combination of chemical and physical etching, only the wet chemical etch process is discussed [26,27]. Wet etch, also known as a chemical etch, is the process in which material is removed via a chemical reaction between the material to be removed and the solution it is submersed in. Since chemical etches have a higher selectivity in comparison to physical etches, it is able to remove a material without removing the underlying material. Wet etches are also highly isotropic, thus limiting the minimum device dimensions that can be achieved.

The process begins by patterning a deposited film via photolithography and then submersion in a liquid etchant. Chemical etching is used to pattern the channel layer for devices used for investigating contact resistance. The channel layer is etched using a solution hydrochloric acid (HCl) diluted with de-ionized water.

3.1.2.4 Lift-off technique

While etching is a subtractive process, lift-off is an additive process. Material is deposited onto a surface where photoresist is not present. Lift-off is used when an etch process is not viable. This technique begins by patterning the substrate via photolithography, a film is then deposited on top of the photoresist layer, and lastly, the entire substrate is submersed in acetone to remove the underlying photoresist layer and the unwanted deposited material. While the photoresist is soluble in acetone, the deposited material is not, resulting in the material deposited on top of the photoresist to be lifted-off the

substrate, leaving only the desired pattern. The use of an ultrasonic cleaner is needed in the event that the material is not removed completely by the acetone soak. Since the photoresist is spun on before the deposition of a material, there is the possibility of contamination between deposited films.

The lift-off process is used to pattern the source and drain contacts for devices fabricated for investigation of contact resistance. ITO is deposited as the source and drain electrode material and soaked for an hour in an acetone bath, followed by 30 seconds in an ultrasonic cleaner to remove residual ITO. Figure 3.3 compares and contrasts etching and lift-off processes.

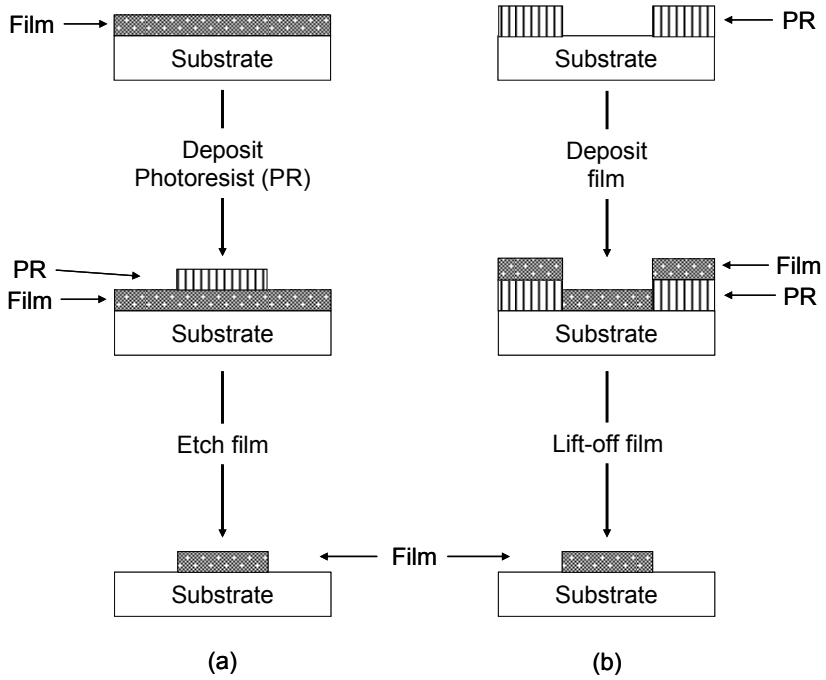

Figure 3.3: Comparison between (a) etching, a subtractive process, and (b) lift-off, an additive process.

3.1.3 Post-deposition anneal

Post-deposition anneal is an important step in the fabrication of transistors. The general purpose of a post-deposition anneal is to improve remove defects created during processes such as ion implantion and sputtering. For the purpose of this thesis research, post-deposition annealing is used to improve device performance. A furnace anneal in air fills oxygen vacancies present in the thin-film

after deposition, removes defects created by the sputtering process, and improves the local atomic order, which improves the channel mobility, and ultimately the overall device performance.

Furnace anneal in air is employed throughout this research with anneal temperatures ranging from 200 to 800 °C.

3.2 DC electrical characterization

Electrical characterization is used to assess device performance. This section discusses the techniques used in assessing contact resistance and material stability. Contact resistance can be extracted from various techniques; the method employed in this thesis, is the method defined by Terada *et al.* [15].

There are three main figures-of-merit for TFT performance: turn-on voltage, drain current on-to-off ratio, and channel mobility, as discussed previously in Chapter 2. These merits are used in assessing instabilities in TFTs. Data presented in this thesis is obtained using Cascade RF-1 with DC probes connected to a HP 4156B Semiconductor Parametric Analyzer with high resolution sense/measure units.

3.2.1 Contact resistance

Contact resistance is an important parameter as it can affect device performance. Two structures are available for determining contact resistance: transistor and transmission line (TLM) structures. Extraction methods using these structures are discussed in detail in this section.

3.2.1.1 Transistor structure

The method described by Terada *et al.* is commonly used to determine the series resistance and the effective channel length of a device under test (DUT) [15]. Series resistance, more commonly called measured resistance, R_M, is the resistance seen between the source and the drain of a transistor. It is comprised of the source resistance, R_S, the channel resistance, R_{CH}, and also the drain resistance, R_D. The total contact resistance, R_{SD}, is the sum of the resistance seen by R_S and R_D; $R_{SD} = R_S + R_D$. The

source and drain resistances (shown in Fig. 3.4) are more complex in that they also include spreading resistance from the probe to the channel and sheet resistance from the contact electrodes. The effective channel length, L_{eff}, is an electrical parameter that differs from the drawn gate length, L, which is taken from the dimensions of the masks used to fabricate devices,

$$L_{eff} = L - \Delta L \,. \tag{3.1}$$

In an ideal MOSFET, L_{eff} is the approximate distance between the space charge regions in the source and drain wells that have encroached under the gate, as shown in Fig. 3.5. In a TFT, the channel length may differ due to processing variations, over-etching, improper lift-off, as well as current crowding under the source/channel and drain/channel overlap regions.

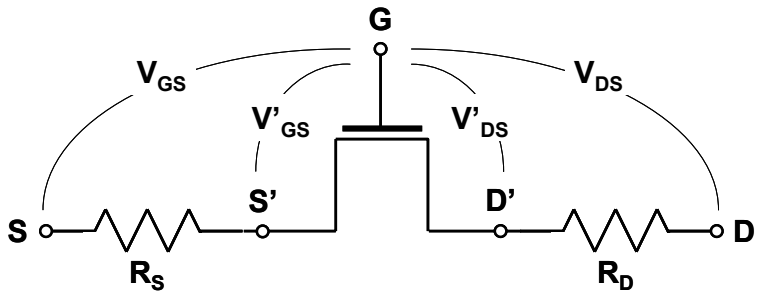

Figure 3.4: Schematic showing an intrinsic transistor with a lumped parameter representation of the source and drain resistances.

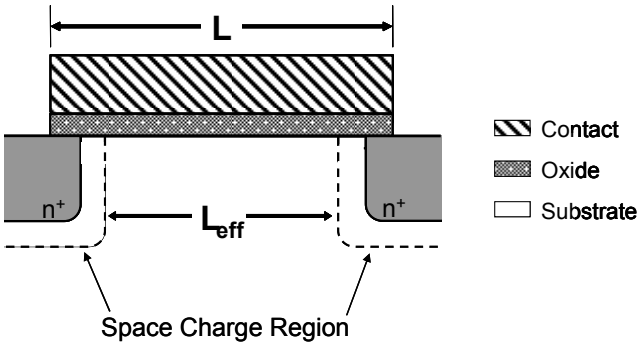

Figure 3.5: Device cross-section for a MOSFET showing the drawn gate length, L, and the effective channel length, L_{eff}, where $L_{eff} = L - \Delta L$.

The current equation for a transistor operating in the linear regime is used to extract R_{SD} and ΔL. The equation shown below is similar to Eq. 2.1, where V_{GS} and V_{DS} have been replaced by V'_{GS} and V'_{DS} in accordance with Fig. 3.4, and W and L have been replaced by W_{eff} and L_{eff}, respectively, resulting in

$$I_D = \frac{(W - \Delta W)\mu_{eff} C_{OX}}{L - \Delta L}\left(V'_{GS} - V_{ON} - V'_{DS}\right)V'_{DS}, \tag{3.2}$$

where $V'_{GS} = V_{GS} - I_D R_S$ and $V'_{DS} = V_{DS} - I_D(R_S + R_D)$. Since $R_{SD} = R_S + R_D$, and $R_S = R_D = \frac{R_{SD}}{2}$, Eq. 3.2 can be rewritten as

$$I_D = \frac{(W - \Delta W)\mu_{eff} C_{OX}}{L - \Delta L}\left[\left(V_{GS} - V_{ON} - \frac{V_{DS}}{2}\right)\left(V_{DS} - I_D R_{SD}\right)\right]. \tag{3.3}$$

When $V_{DS}/2 << V_{GS} - V_{ON}$, $V_{DS}/2$ becomes negligible since $V_{GS} - V_{ON}$, dominates. Thus, Eq. 3.3 becomes

$$I_D = \frac{(W - \Delta W)\mu_{eff} C_{OX}}{L - \Delta L}\left[\left(V_{GS} - V_{ON}\right)\left(V_{DS} - I_D R_{SD}\right)\right], \tag{3.4}$$

which can be rewritten as

$$I_D = \frac{(W - \Delta W)\mu_{eff} C_{OX}\left(V_{GS} - V_{ON}\right)V_{DS}}{(L - \Delta L) + (W - \Delta W)\mu_{eff} C_{OX}\left(V_{GS} - V_{ON}\right)R_{SD}}. \tag{3.5}$$

Given Ohm's Law, V = IR, Eq. 3.5 can be rearranged such that R_M is defined as follows,

$$R_M = \frac{V_{DS}}{I_D} = R_{CH} + R_{SD}$$

$$= \frac{(L - \Delta L)}{(W - \Delta W)\mu_{eff} C_{OX}\left(V_{GS} - V_{ON}\right)} + R_{SD}. \tag{3.6}$$

The approach used by Luan and Neudeck, where the measured resistance is normalized by the channel width can be applied to Eq. 3.6, which becomes

$$R_M \cdot W_{eff} = \frac{V_{DS} \cdot W_{eff}}{I_D} = \frac{(L - \Delta L)}{\mu_{eff} C_{OX}\left(V_{GS} - V_{ON}\right)} + R_{SD} \cdot W_{eff} \tag{3.7}$$

This equation is of the form $y = m(x-x_o) + b$ with $R_M \cdot W_{eff}$, L, and ΔL, corresponding respectively to y, x, and x_o. Thus, $R_M \cdot W_{eff} = R_{SD} \cdot W_{eff}$ when $L = \Delta L$, so that both R_{SD} and ΔL can be easily extracted, as illustrated by Fig. 3.6. Contact resistance is determined by R_{SD}, while ΔL is used in assessing L_{eff}.

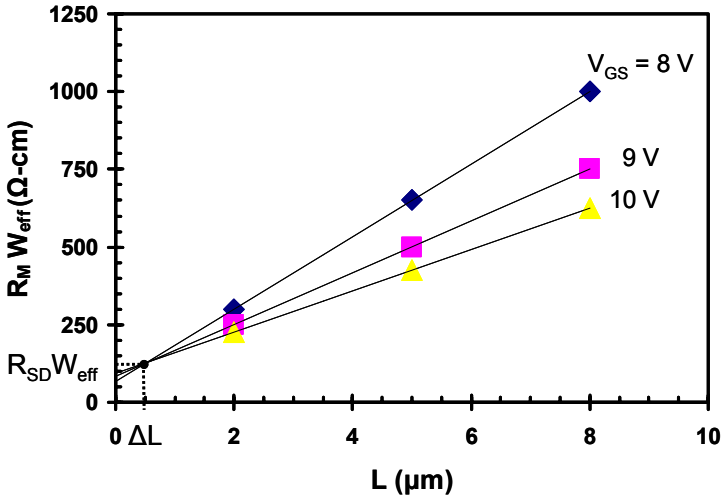

Figure 3.6: Idealized data set used to demonstrate the extraction of contact resistance from a transistor structure. Normalized measured resistance, $R_M \cdot W_{eff}$ is ploted versus channel length, L, as a function of gate voltage. $R_{SD} \cdot W_{eff}$ and ΔL are estimated from the point at which the lines cross.

3.2.1.2 Transmission line structure

The transfer line method (TLM) test structure (Fig. 3.7) gives rise to another method for extracting R_{SD}. While TLMs are typically used to determine the contact resistance of a conducting material, a gated-TLM structure is required for insulating channel materials. The technique used to extract parasitic resistance for a conducting material is first presented, followed by a discussion for extracting contact resistance for a semiconducting material.

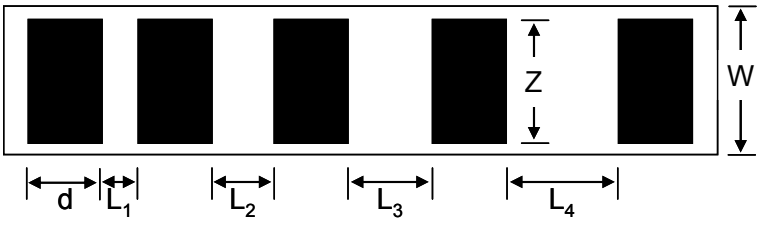

Figure 3.7: A transfer line method (TLM) test structure.

The resistance measured between any two contact pads is denoted as the total resistance, R_T [15]. The total resistance is a function of the sheet resistance, ρ_s, the width of the contact, Z, the spacing between contacts, L, and also the contact resistance. R_T can be expressed as a function of ΔL [15],

$$R_T = \frac{\rho_s L}{Z} + R_{SD} \approx \frac{\rho_s}{Z}(d + \Delta L) \tag{3.8}$$

Equation 3.8 is of the form $y = m(x + x_o)$ with ρ_s/Z, L, and ΔL corresponding, respectively, to m, x, and x_o. Thus, $R_T = R_{SD}$ when d = 0 and $-d = \Delta L$ when $R_T = 0$ so that both R_{SD} and ΔL may be estimated, as illustrated by Fig. 3.8.

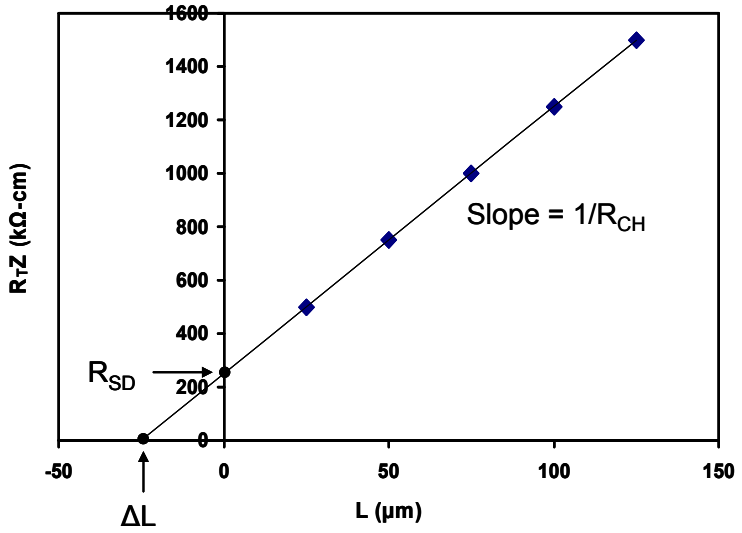

Figure 3.8: Idealized data set used to demonstrate the extraction of contact resistance from a TLM structure. Normalized total resistance, $R_T \cdot Z$, plotted as a function of contact spacing, L. R_{SD} is estimated as the x-axis intercept, ΔL is estimated as the y-axis intercept, and the slope is $1/R_{CH}$, where R_{CH} is the channel resistance.

The TLM method can be applied to the assessment of insulating channel layers used in TFTs if a bottom gate is used to induce electrons into the channel. Varying gate voltages are applied and $R_T \cdot Z$ is plotted versus L, as a function of V_{GS}, as shown in Fig. 3.9. R_{SD} and ΔL are estimated from the point at which the lines intersect. This technique is employed in publications by Martin *et al.* and Kanicki *et al.* [18,25]

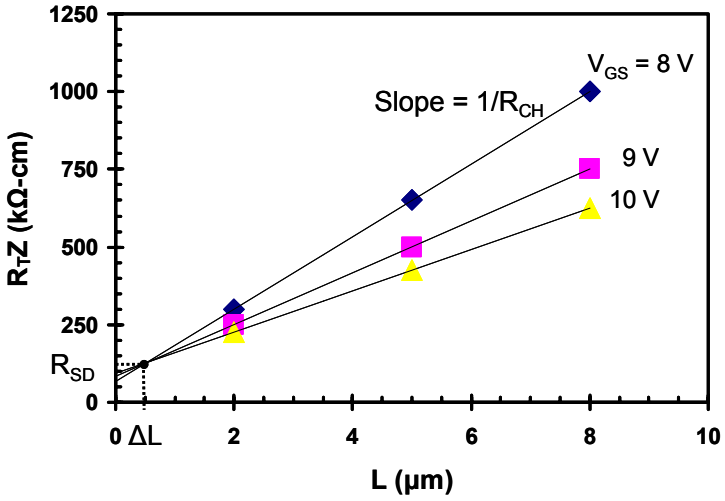

Figure 3.9: Idealized data set used to demonstrate the extraction of contact resistance from a TLM structure of an insulating channel layer using a bottom-gate to induce electrons into the channel. Normalized total resistance, $R_T \cdot Z$, plotted versus contact spacing, L, as a function of gate voltage. R_{SD} and ΔL are estimated from the point at which the lines intersect. V_{GS} refers to the voltage applied to the bottom-gate.

3.2.1.2 Device performance

As previously mentioned, contact resistance can affect device performance. To assess the effect of contact resistance when ITO is used as a contact to wide-band gap semiconductors, the mobility of a TFT is monitored.

Mobility estimates are extracted from a transfer curve which is obtained by setting V_{DS} at a low voltage (1 V) and sweeping the gate voltage. The range of the gate voltage sweep is adjusted according to material and dielectric properties. In Fig. 3.10, the gate is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 1 V. The data obtained from this sweep is then used to calculate average and incremental mobility (refer to Section 2.1.2) as a function of V_{GS}. Figure 3.11 shows typical mobility trends as a function of V_{GS}. Contact resistance for specific material systems (ZnO, ZIO, and IGO) is explored in detail in Chapter 4.

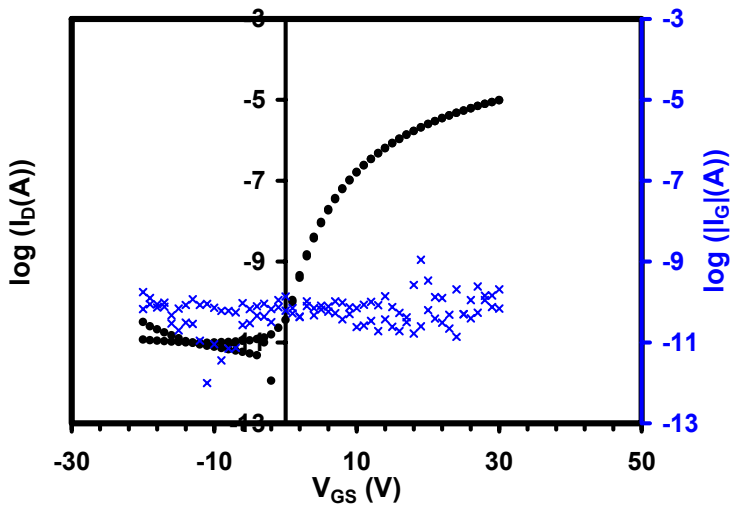

Figure 3.10: log(I_D)-V_{GS} transfer curve for mobility extraction. The gate bias is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 1 V. The DUT is a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm.

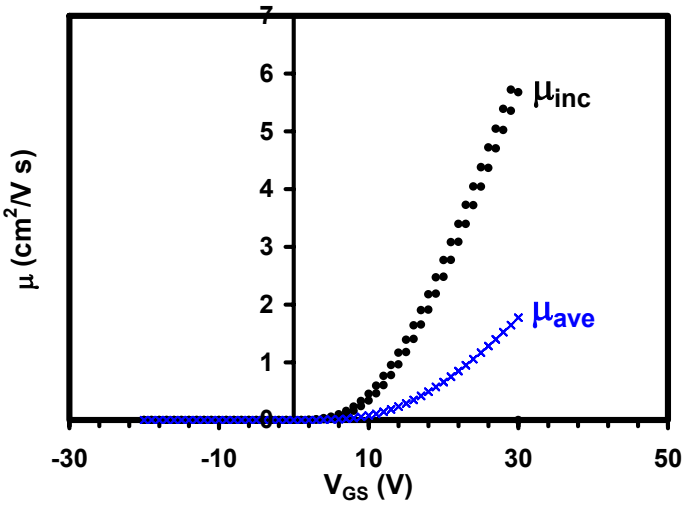

Figure 3.11: Mobility as a function of gate voltage. Data obtained in Fig 3.9 is used calculate both the incremental mobility, μ_{inc}, and the average mobility, μ_{ave}. In this example, the maximum value of μ_{inc} and μ_{ave} are 5.7 and 1.8 cm^2/V-s, respectively. The DUT is a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm.

3.2.2 Stability assessment

Reliability is a crucial factor if a material is to be manufactured on a large scale for applications such as circuits. The purpose of this work is to determine if instabilities are present in a channel material used in an oxide-based TFT. The methodology for stability assessment is outlined in detail in the remainder of this section.

The stability assessment methodology is threefold: criterion selection, implementation of testing strategy, and data analysis.

First, a criterion for determining if a material and/or device is stable must be specified. As previously mentioned in Section 2.4, the criteria utilized in this thesis for assessing stability in an oxide-based thin-film transistor are a shift in V_{ON}, a change in I_D, and a change in the peak channel mobility.

Second, a testing strategy based on the established criteria is implemented to collect the necessary data. The testing strategy developed in the context of this research is comprised of three steps.

Step 1: Characterization suite to collect initial data. A characterization suite is the phrase coined to encompass the three basic curves collected and used in evaluating device performance. These

basic curves are the transfer curve $\log(I_D)$ - V_{GS} at small V_{DS} (~ 1 V) for mobility extraction, the transfer curve $\log(I_D)$-V_{GS} at larger V_{DS} (~ 20–30 V) for I_{ON-OFF} extraction, and the output curve, I_D-V_{DS}. The transfer curves and output curve are swept in both forward and reverse directions for quantitative hysteresis assessment; the sweep rate for the curves is ~ 1 V/s. The transfer curve for mobility extraction is obtained by setting V_{DS} at a low voltage (1 V) and sweeping the gate voltage. The gate voltage sweep is adjusted according to material and dielectric properties. In Fig. 3.10, the gate is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 1 V. The data obtained from this sweep is then used to calculate average and incremental mobility (refer to Section 2.1.2) as a function of V_{GS}. Figure 3.11 shows typical mobility trends as a function of V_{GS}. The transfer curve for I_{ON-OFF} extraction, illustrated by Fig. 3.12, is obtained by setting V_{DS} high (~ 20 – 30 V) and sweeping the gate bias. The output curve is a good measure of current drive and a quick way to observe if the DUT exhibits acceptable transistor behavior, as discussed in Section 2.1.1. The output curve is obtained by sweeping both V_{DS} and V_{GS}. The gate bias sweep can be adjusted according to material and dielectric properties. Figure 3.13 shows the output curve for a DUT.

Step 2: Repeat characterization suite. This second characterization suite serves as an assessment of the short-term reliability of a device and acts as a stabilization step for the DUT in the event that the device is not initially stable and requires a “burn-in” step.

Step 3: Bias testing with constant voltage applied to the DUT. In this step, V_{GS} and V_{DS} are held constant while the drain current is monitored. I_D as obtained from the “square law” theory is given as

Changes ? Held constant

$$I_D = \frac{1}{2}\frac{\mu C_{ox} W}{L}\left(V_{GS} - V_{ON}\right)^2. \qquad (2.1)$$

Monitor Changes ?

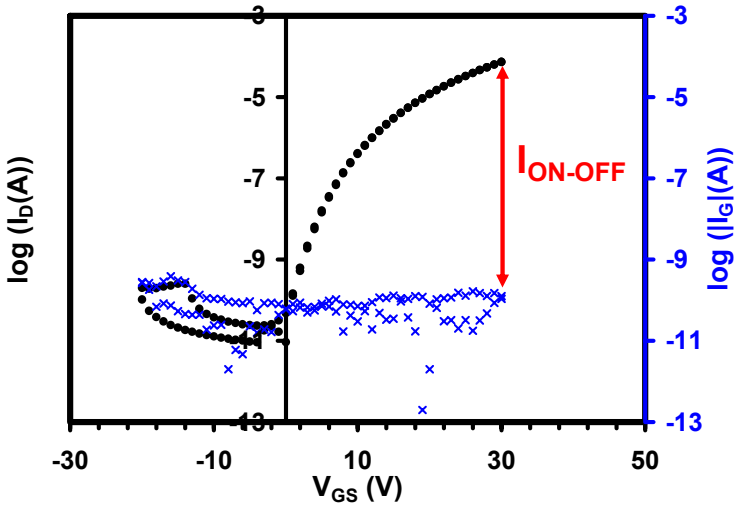

Figure 3.12: $\log(I_D)$-V_{GS} transfer curve for $I_{ON\text{-}OFF}$ extraction. The gate bias is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 30 V. $I_{ON\text{-}OFF}$ is greater than 10^6. The DUT is a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 µm.

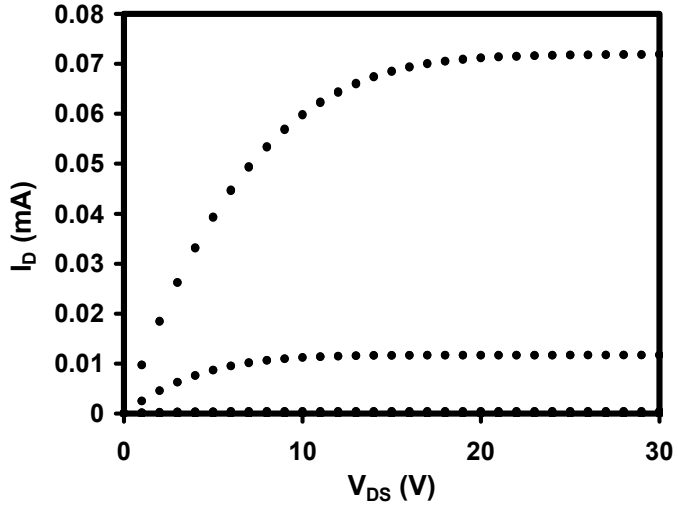

Figure 3.13: I_D-V_{DS} output curve for a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 µm. 0 V ≤ V_{DS} ≤ 30 V in 1 V steps and -20 V ≤ V_{GS} ≤ 30 V in 10 V steps (I_D increases with increasing V_{GS}).

As evident from Eq. 2.1, a change in I_D could be the result of a change in either V_{ON} and/or μ. Bias testing is also referred to as stress testing since current flows through the device over an extended period of time. The purpose of stressing is to determine if changes in device performance occur during long-term operation. Bias testing of the DUT is interrupted at time intervals of 10^3 s, 10^4 s, and 10^5 s to obtain device performance data by running the characterization suite. A full characterization data set requires approximately 4-5 minutes, thus adding minimal time delay to the stressing process. The data collected in Steps 1 and 2 are considered to be taken at t = 0 s, and t = 0^+ s, i.e., "+" denotes minimal time elapse from t = 0 s, respectively. A bias stress plot of I_D versus time is shown in Fig. 3.14 for a DUT under bias stressing.

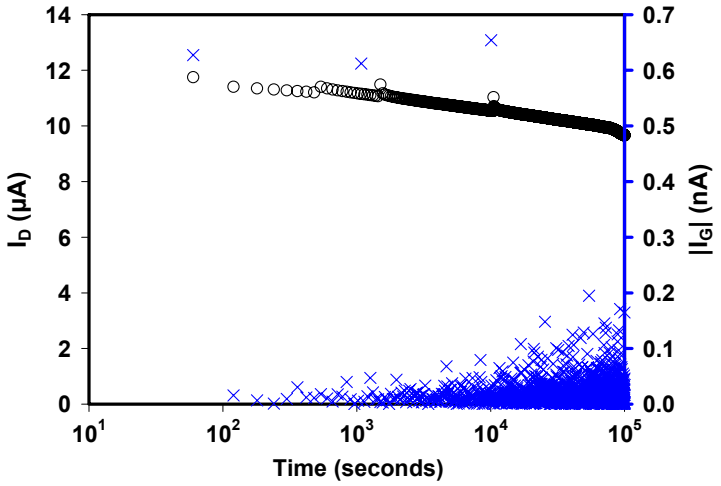

Figure 3.14: I_D-time plot for a TFT under bias stress testing. The TFT is composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm. Sampling parameters: V_{GS} = 20 V, V_{DS} = 20 V, and time taken at intervals of 1 second.

Finally, a bias stress measurement is completed by analyzing the data collected. The data is presented as shown in Table 3.1, such that trends can be identified in V_{ON}, I_D, and the peak mobilities and ultimately determine the stability of the channel layer material. Data analysis is discussed in detail for each material system (ZnO, ZIO, and IGO) in Chapter 5.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (μA) @ $V_{DS} = V_{GS} = 30$ V
0	-2	5.7	10^6	71.9
0^+	-2	5.7	10^6	71.6
10^3	-2	5.6	10^6	70.4
10^4	-3	5.5	10^6	68.4
10^5	-2	5.4	10^6	64.7

Table 3.1: Summary of a bias stress measurement for a TFT composed of a ZnO channel layer (~ 50 nm) and a thermal silicon oxide as the gate insulator; W/L = 5 with L = 200 μm.. No shift in V_{ON} resulted after the stressing process. Peak mobilities and drive current, I_D, are slightly decreased.

3.3 Conclusions

In this chapter, deposition methods and techniques relevant to the research conducted for this thesis are presented. Fabrication techniques such as PVD processes, patterning techniques, and post-deposition annealing are discussed. An electrical characterization methodology for determining contact resistance and assessing TFT instabilities is also explored.

4. EFFECT OF CONTACT RESISTANCE ON OXIDE-BASED THIN-FILM TRANSISTORS

This chapter focuses on implementation of the methodology discussed in Chapter 3, Section 3.2.2 for assessing the effect of contact resistance on the performance of oxide-based TFTs. Device fabrication is also presented.

4.1 Device fabrication

Devices used for this research are staggered, bottom-gate TFTs and TLM structures, which are both fabricated on either 1 x 1 inch silicon substrates with thermally grown SiO_2 or on 1 x 1 inch glass substrates coated with ITO and ATO. For the silicon substrates, the gate dielectric is a 100 nm thick thermally grown SiO_2 on top of a p-type Si wafer. After SiO_2 is etched from the backside of the wafer, tantalum (Ta) and gold (Au) are deposited; Ta (10 nm) serves as an adhesion layer between the Au (300 nm) and silicon substrate. The substrates with thermal oxide and Au/Ta are supplied by the Hewlett-Packard Company. The Si/Ta/Au stack constitutes the gate contact.

The glass substrates are coated with 200 nm sputtered ITO and a 220 nm thick layer of aluminum titanium oxide (ATO) deposited via atomic layer deposition. ITO acts as the gate electrode and the ATO layer acts as the gate insulator and is comprised of a superlattice of alternating Al_2O_3 (aluminum oxide) and TiO_2 (titanium oxide) layers. The glass substrate ATO and ITO are manufactured by Nippon Sheet Glass Company and supplied by Planar Systems, Inc.

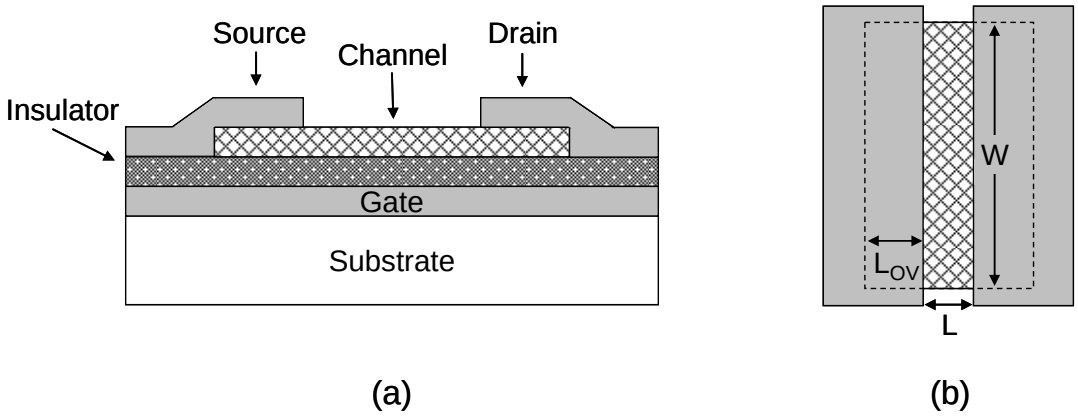

Figure 4.1: (a) Cross-section and (b) plan-view of a bottom-gate TFT, where L is the channel length, W is the channel width, and L_{OV} is the overlap distance between the channel and electrode.

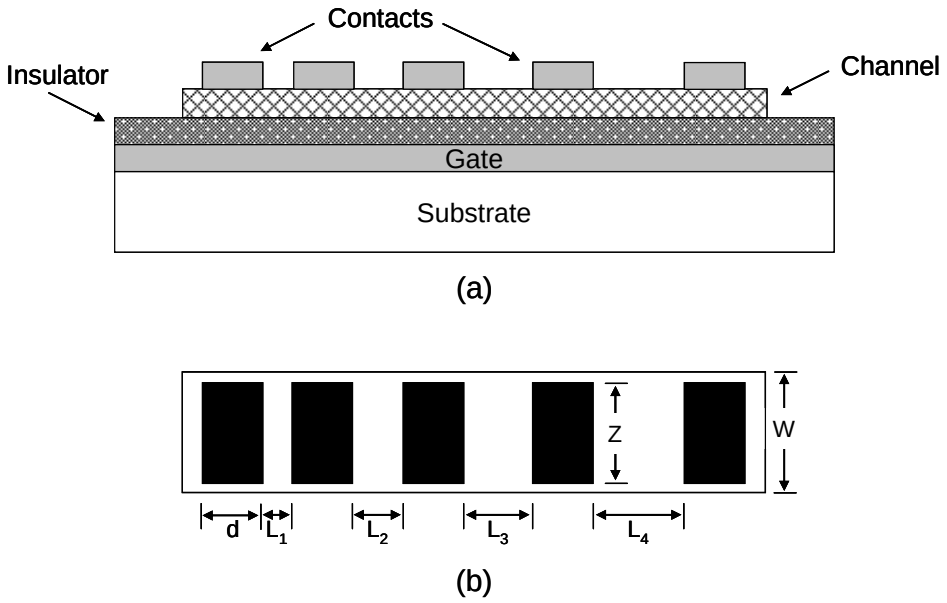

Figure 4.2: (a) Cross-section and (b) plan-view of a TLM structure, where L is the contact length, W is the channel width, Z is the contact width, and d is the spacing between contact pads.

The fabrication process consists of five steps, two which are photolithography steps using mylar masks (CAD/Art Services, Inc.). A cross-section and a plan view of a TFT and a TLM structure are shown in Figs. 4.1 and 4.2.

1. The channel layer (~ 50 nm) is deposited via RF magnetron sputtering from a 2 inch target (Cerac, Inc.; ZnO and IGO (1:1 molar ratio of In_2O_3:Ga_2O_3)) at a pressure of 5 mTorr, power density of ~ 2.5 W/cm^2 for ZnO and ~ 3.7 W/cm^2 for IGO, a target-to-substrate distance of ~ 10.2 cm, and no intentional substrate heating. Process parameters for ZnO and IGO are tabulated in Table 4.1.
2. Mask 1: The channel is defined using an HCl wet etch. Molar ratio and etch rates for the different channel materials are listed in Table 4.2. TFTs have dimensions W = 250, 500, 1250 μm. L = 50, 100, 200 μm, and L_{OV} = 25, 50, 100 μm. TLM structures have dimensions W = 300 μm, L = 50 μm, Z = 297.5 μm, and d = 25, 50, 75, 100, and 125 μm.
3. The sample is subjected to a 600 °C furnace anneal in air for one hour.
4. Mask 2: Source/drain contacts are deposited by ion beam sputtering from an ITO target in Ar/O_2 ambient (80%/20%) at 10^{-4} Torr without intentional substrate heating. Patterning is accomplished through photolithography and lift-off.

Channel Material	Ambient (Ar/O_2)	Pressure (mTorr)	Power Density (W/cm^2)	Target-Substrate-Distance (cm)	T_{Anneal} (°C)	Thickness (nm)
ZnO	90%/10%	5	~ 2.5	~ 10.2	600	~ 50
IGO (1:1, In_2O_3:Ga_2O_3)	90%/10%	5	~ 3.7	~ 10.2	600	~ 50

Table 4.1: Summary of process parameters for TFTs fabricated on thermal silicon oxide and furnace annealed.

Channel Material	Wet Etch	Etch Rate
ZnO	~ 0.01 M HCl	~ 17.5 Å/s
IGO (1:1, In_2O_3:Ga_2O_3)	~ 2 M HCl	~ 6.3 Å/s

Table 4.2: Summary of etch parameters for ZnO and IGO channel materials.

4.2 Electrical characterization

Contact resistance is evaluated for ITO when it is used as a contact to ZnO and IGO. The effect of contact resistance on device performance, specifically channel mobility and turn-on voltage, is also investigated.

4.2.1 TFT structures

Measured resistance normalized by the channel width, $R_M \cdot W$, plotted versus channel length, L, and as a function of gate voltage is shown in Figs. 4.3 and 4.4 for ZnO TFTs fabricated using thermal silicon oxide and ATO gate insulators, respectively. $R_M \cdot W$ is collected at V_{DS} = 0.5 V with the gate swept from 20 V ≤ V_{GS} ≤ 25 V. ZnO TFTs fabricated using SiO_2 (Fig. 4.3) yield $R_{SD} \cdot W \sim 0$ kΩ-cm. It is observed that ΔL is a function of L_{OV}; as L_{OV} increases, ΔL decreases, as summarized in Table 4.3. Figure 4.4 shows data for ZnO TFTs fabricated using ATO as the gate dielectric. $R_{SD} \cdot W$ is in the range of 0.7-3.5 kΩ-cm. No trend in ΔL is observed for this material system. Note that ΔL is negative for devices fabricated using SiO_2, but positive for TFTs fabricated using ATO.

The channel resistance as of function of V_{GS}, R_{CH} (V_{GS}), can be extracted from Fig. 4.3 where the inverse of the slope of $R_M \cdot W$ versus L gives $R_{CH} \cdot W$. For the ZnO TFT on thermal silicon oxide (Fig. 4.3(a)), at V_{GS} = 20 V, $R_{CH} \cdot W \sim 4.6$ kΩ-cm. For contact resistance to be considered negligible,

$$R_{SD} \cdot W << R_{CH} \cdot W \ . \tag{4.1}$$

Thus, since $R_{SD} \cdot W \sim 0$ kΩ-cm and $R_{CH} \cdot W \sim 4.6$ kΩ-cm, the contact resistance is negligible in comparison to the channel resistance for these devices. However, the contact resistance for ZnO TFTs fabricated using ATO is not negligible, since it is found to be $R_{SD} \cdot W$ = 0.7-3.5 kΩ-cm compared to the extracted channel resistance at V_{GS} = 20 V which is estimated as approximately 1.3 kΩ-cm.

TFTs fabricated using IGO as the channel material and thermal silicon oxide as the gate insulator are presented in Fig. 4.5. $R_M \cdot W$ is collected at V_{DS} = 1 V with the gate swept from 5 V ≤ V_{GS} ≤ 10 V. $R_{SD} \cdot W$ is found to range from ~ 0.05 to 0.15 kΩ-cm, with no observable trend in ΔL.

Compared to the channel resistance extracted at V_{GS} = 5 V for IGO TFTs with L_{OV} = 25 µm (Fig. 4.3(a)), R_{CH} is ~ 6.2 kΩ-cm, while R_{SD}·W is in the range of 0.05 - ~ 0.15 kΩ-cm. It can be concluded that the contact resistance for IGO TFT structures is negligible.

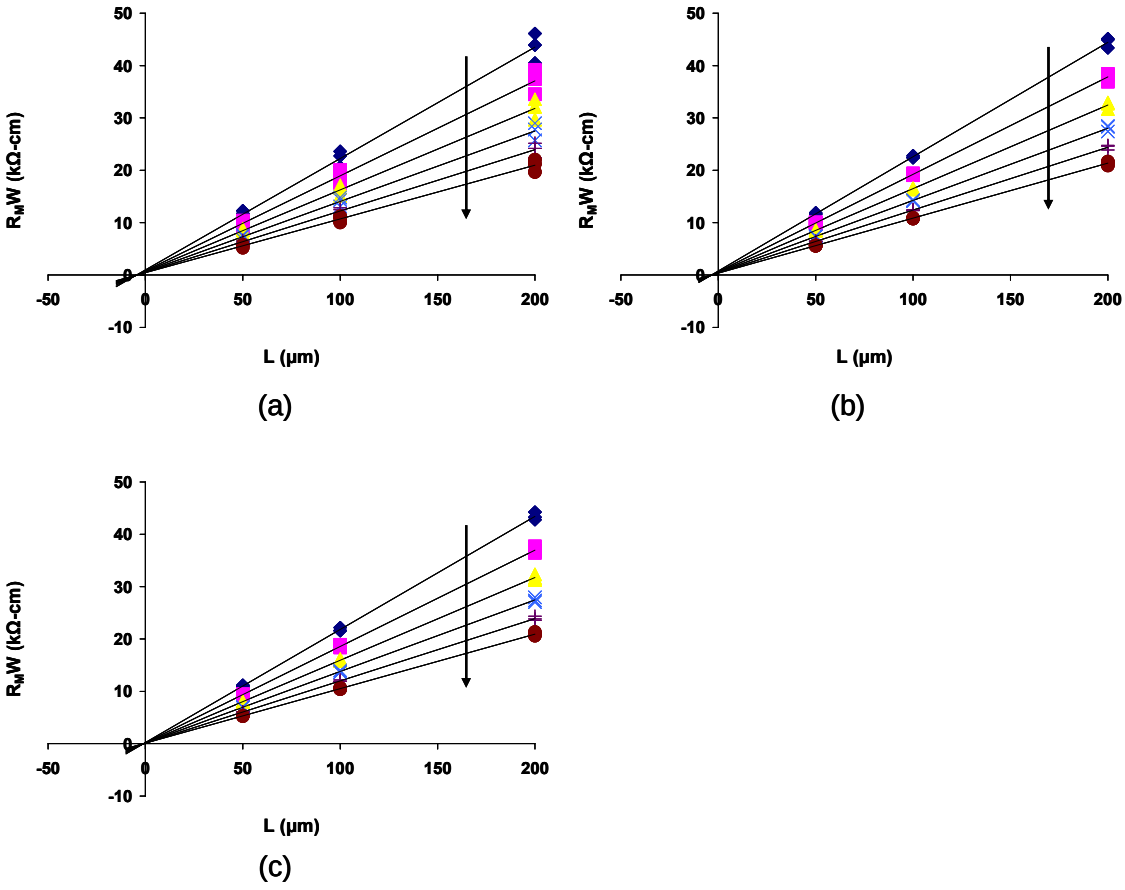

Figure 4.3: Measured resistance normalized by channel width, R_M·W, as a function of channel length, L, for ZnO TFTs fabricated on thermal silicon oxide with (a) L_{OV} = 25 µm, (b) L_{OV} = 50 µm, and (c) L_{OV} = 100 µm. R_M·W is collected at V_{DS} = 0.5 V and 20 V ≤ V_{GS} ≤ 25 V in 1 V steps; arrow is in direction of increasing V_{GS}.

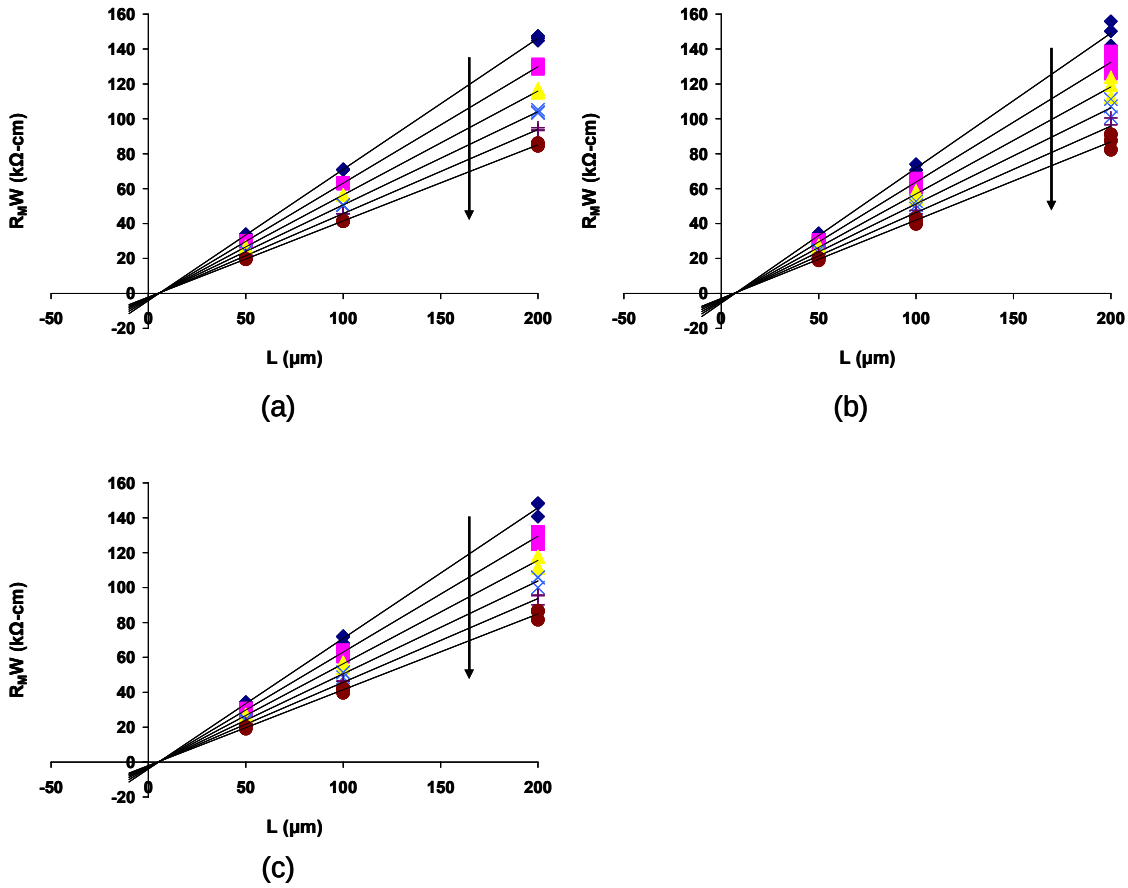

Figure 4.4: Measured resistance normalized by channel width, $R_M \cdot W$, as a function of channel length, L, for ZnO TFTs fabricated on ATO with (a) L_{OV} = 25 μm, (b) L_{OV} = 50 μm, and (c) L_{OV} = 100 μm. $R_M \cdot W$ is collected at V_{DS} = 0.5 V and 20 V ≤ V_{GS} ≤ 25 V in 1 V steps; arrow is in direction of increasing V_{GS}.

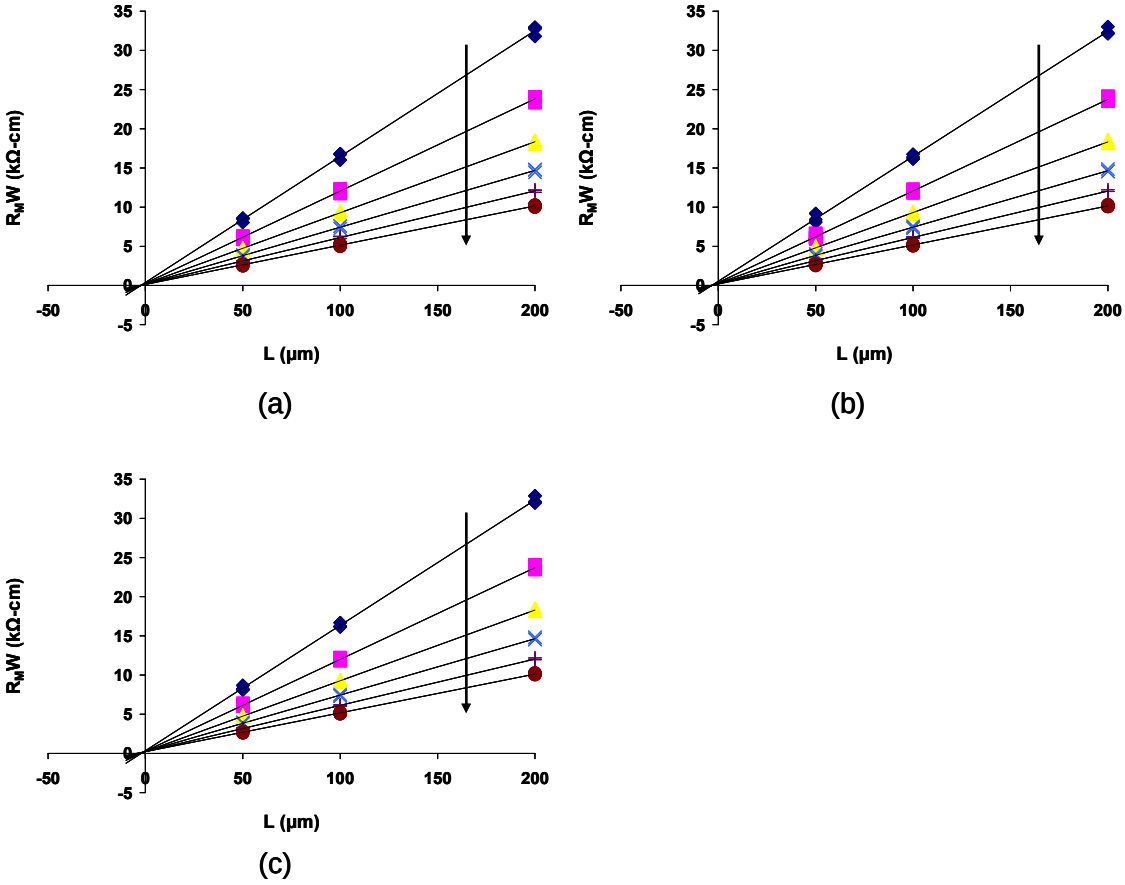

Figure 4.5: Measured resistance normalized by channel width, $R_M \cdot W$, as a function of channel length, L, for IGO TFTs fabricated on thermal silicon oxide with (a) L_{OV} = 25 µm, (b) L_{OV} = 50 µm, and (c) L_{OV} = 100 µm. $R_M \cdot W$ is collected at V_{DS} = 1 V and 5 V ≤ V_{GS} ≤ 10 V in 1 V steps; arrow is in direction of increasing V_{GS}.

Contact resistance measurements for all three material systems evaluated, i.e., ZnO/SiO2, ZnO/ATO, and IGO/SiO_2, are summarized in Table 4.3. Negligible contact resistance is found in transistor structures fabricated using SiO_2, while the contact resistance is non-negligible for ZnO TFTs fabricated on ATO. A relationship between ΔL and L_{OV} is observed for ZnO/SiO_2 TFTs, where ΔL decreases as L_{OV} increases. However, this same trend is not present for TFTs fabricated using ZnO/ATO and IGO/SiO_2 material systems. The variation in ΔL may be attributed to data variation.

Material	L_{OV} (μm)	R_{SD}·W (kΩ-cm)	R_{CH}·W (kΩ-cm)	ΔL (μm)
ZnO on SiO_2	25	~ 0	~ 4.6 @ V_{GS} = 20 V	~ -5
	50	0		-3.5
	100	0		-1
ZnO on ATO	25	3.5	~ 1.3 @ V_{GS} = 20 V	6
	50	0.7		8
	100	3.5		6
IGO on SiO_2	25	0.05	~ 6.2 @ V_{GS} = 5 V	-2
	50	~ 0.05		-3
	100	0.15		-1

Table 4.3: Summary of contact resistance measurements for ZnO and IGO TFTs fabricated on thermal silicon oxide and ZnO TFTs fabricated using ATO gate dielectric furnace annealed at 600 °C for varying overlap distances, L_{OV}.

4.2.2 TLM structure

As presented in Section 3.2.1, a TLM test structure is another method used for extracting contact resistance. In general, the TLM method is used to determine the contact resistance to conducting materials. However, in this work, the TLM test structure is employed to measure the contact resistance of an insulating channel layer with a bottom-gate used to induce electrons into the channel. The extraction of R_{SD} in these gated structures differs slightly from conventional TLM methodology since the measurement is performed at various gate voltages. Total resistance normalized by the contact width, R_T·Z is plotted versus L, as a function of V_{GS}.

Figure 4.5 shows total resistance normalized by contact width, R_T·Z, plotted versus the contact spacing, L, as a function of gate voltage. R_T·Z is collected at V_{DS} = 0.5 V with the gate swept from 20 V ≤ V_{GS} ≤ 25 V. R_T·Z and ΔL for ZnO TLMs fabricated using thermal silicon oxide (Fig. 4.6(a)) are

found to be in the range of 0-3 kΩ-cm and -5-(-15) μm, respectively. Data obtained from a ZnO TLM fabricated with ATO as a gate insulator are shown in Fig 4.6(b), yielding $R_T \cdot Z \sim 0.5$ kΩ-cm and $\Delta L \sim 6$ μm. The channel resistance normalized by contact width, $R_{CH} \cdot Z$, extracted at $V_{GS} = 5$ V is 4.7 and 1.2 kΩ-cm for ZnO TFTs fabricated using SiO_2 and ATO, respectively. Note that unlike the other data sets presented in this thesis, the data obtained for the ZnO TLM structure does not precisely fit a linear curve, indicating that this data set is less reliable in comparison to the others. This non-linearity is persistent with repeated tests for an undetermined reason.

Contact resistance measurements of a TLM structure fabricated using an IGO channel layer and thermal silicon oxide as a gate insulator are presented in Fig. 4.7. $R_T \cdot Z$ is collected as $V_{DS} = 1$ V with the gate swept from 5 V ≤ V_{GS} ≤ 10 V. $R_T \cdot Z$ and ΔL are extracted to be 0.2 kΩ-cm and ~ 1.5 μm, respectively. The contact resistance is negligible with respect to the channel resistance, which is ~ 6.3 kΩ-cm.

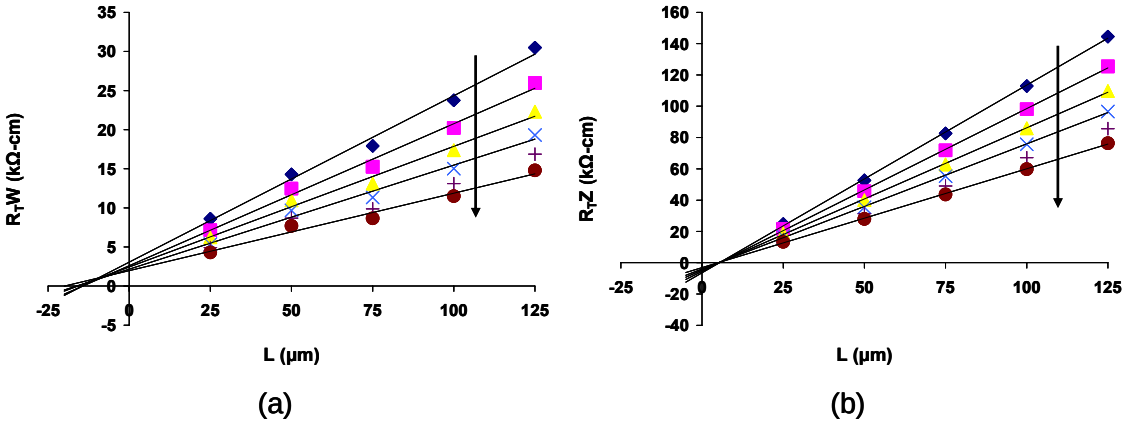

Figure 4.6: Total resistance normalized by contact width, $R_T \cdot Z$, as a function of contact spacing, L. TLM structure fabricated with (a) a ZnO channel on thermal silicon oxide and (b) a ZnO channel on ATO. $R_T \cdot Z$ is collected at $V_{DS} = 0.5$ V and 20 V ≤ V_{GS} ≤ 25 V in 1 V steps; arrow is in direction of increasing V_{GS}.

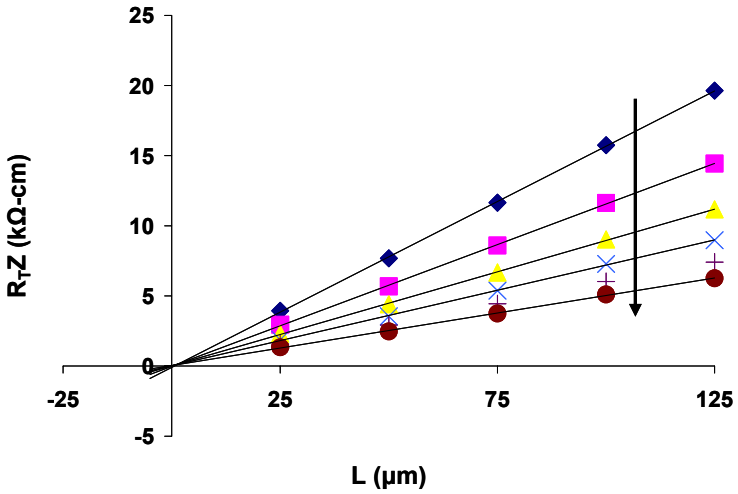

Figure 4.7: Total resistance normalized by contact width, $R_T \cdot Z$ as a function of contact spacing, L. TLM structure fabricated with IGO channel on thermal silicon oxide. $R_T \cdot Z$ collected at V_{DS} = 1 V and 5 V ≤ V_{GS} ≤ 10 V in 1 V steps; arrow is in direction of increasing V_{GS}.

Contact resistance measurements for ZnO/SiO2, ZnO/ATO, and IGO/SiO2 TLM structures are summarized in Table 4.4. Negligible contact resistance is found for IGO/SiO2 TLM strcture, while the contact resistance is indeterminate (too much data variability) or perhaps negligible for the ZnO/SiO2 and ZnO/ATO TLM structures. Note that the results for contact resistance extracted from the ZnO TLM structures contradict the results obtained from ZnO transistor structures. Also ΔL extracted from the IGO TLM is positive, while it was negative for the IGO TFT.

Material	$R_{SD} \cdot Z$ (kΩ-cm)	$R_{CH} \cdot W$ (kΩ-cm)	ΔL (μm)
ZnO on SiO_2	0-3	4.7 @ V_{GS} = 20 V	-5-(-15)
ZnO on ATO	~ 0.5	1.2 @ V_{GS} = 20 V	~ 6
IGO on SiO_2	0.2	6.3 @ V_{GS} = 5 V	~ 1.5

Table 4.4: Summary of contact resistance measurements for ZnO (~ 50 nm) and IGO (~ 50 nm) TLM structures fabricated on thermal silicon oxide and ATO gate dielectric furnace annealed at 600 °C.

4.2.3 Device performance

The purpose of this work is to determine if the contact resistance of ITO on wide-band gap semiconductors effects device performance. Maximum incremental mobility plotted as a function of W/L for ZnO TFTs fabricated on thermal silicon oxide and ATO gate insulators are shown in Fig. 4.8. From Fig. 4.8, the mobility is constant for vary W/L ratios, indication that it is unaffected by the device dimensions used in this work. Note that the mobility for TFTs fabricated using the ZnO/SiO_2 material system averages ~ 4.75 $cm^2/V\text{-}s$, while the mobility for ZnO TFTs fabricated using the ATO gate dielectric averages approximately 1.81 $cm^2/V\text{-}s$. The difference in channel mobility may be explained as a difference in surface roughness between thermal silicon oxide and ATO; the surface roughness for SiO_2 is ~ 0.28 nm whereas ATO is ~ 5.5 nm [28]. It is also observed that the turn-on voltage is also unaffected by device dimensions. Peak incremental mobility and V_{ON} are summarized in Table 4.5.

The mobility is shown an IGO/SiO_2 transistor structures fabricated using SiO_2 in Fig. 4.9. In comparison to the mobility extracted from ZnO TFTs, the mobility extracted from IGO TFTs is scattered; no apparent trends are observed at this time. Further work for this material system is needed. However, the turn-on voltage held steady at approximately 1-2 V for all of the IGO TFTs analyzed, as is summarized in Table 4.5.

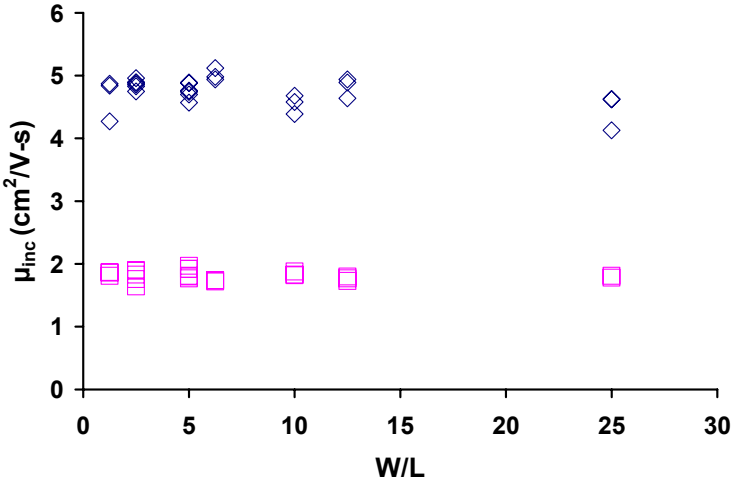

Figure 4.8: Maximum incremental mobility as a function of W/L for ZnO fabricated on SiO_2 (diamonds) and ZnO on ATO (squares).

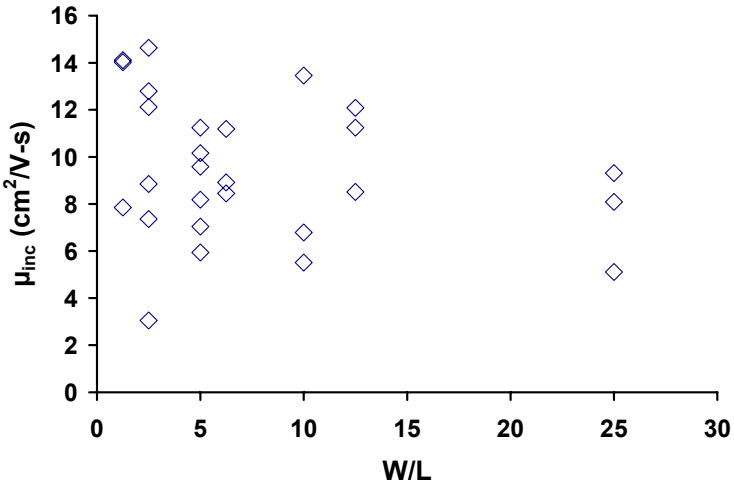

Figure 4.9: Maximum incremental mobility as a function of W/L for IGO (~ 50 nm) TFTs fabricated on SiO_2 and annealed at 600 °C.

Device Dimensions					ZnO/SiO_2		ZnO/ATO		IGO/SiO_2	
Width (μ)	Length (μ)	W/L	S/G Overlap (μ)	D/G Overlap (μ)	μ_{inc} (cm^2/V-s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	V_{ON} (V)
250	50	5	100	100	4.89	-10	1.92	-12	11.24	-1
250	50	5	50	50	4.74	19	1.97	-12	10.16	-1
250	50	5	25	25	4.57	-10	1.92	-13	7.04	-1
250	100	2.5	100	100	4.89	-9	1.89	-12	12.12	-1
250	100	2.5	50	50	4.83	-9	1.9	-12	8.85	-1
250	100	2.5	25	25	4.75	-9	1.83	-12	12.79	-1
250	200	1.25	100	100	4.27	-10	1.87	-11	14.02	-1
250	200	1.25	50	50	4.87	-8	1.86	-11	7.85	-1
250	200	1.25	25	25	4.84	-8	1.81	-11	14.11	-1
500	50	10	100	100	4.68	-10	1.82	-12	6.79	-2
500	50	10	50	50	4.58	-10	1.83	-12	5.51	-2
500	50	10	25	25	4.39	-10	1.88	-12	13.46	-1
500	100	5	100	100	4.88	-9	1.77	-11	8.18	-2
500	100	5	50	50	4.76	-9	1.81	-11	9.58	-1
500	100	5	25	25	4.7	-9	1.8	-11	5.94	-1
500	200	2.5	100	100	4.96	-9	----	----	14.63	-2
500	200	2.5	50	50	4.89	-8	1.64	-10	3.05	-2
500	200	2.5	25	25	4.86	-9	1.76	-10	7.36	-1
1250	50	25	50	50	4.62	-10	1.81	-12	8.09	-1
1250	50	25	25	25	4.13	-10	1.78	-12	9.31	-2
1250	50	25	100	100	4.63	-10	----	-11	5.11	-2
1250	100	12.5	50	50	4.89	-9	1.77	-11	8.51	-2
1250	100	12.5	25	25	4.64	-9	1.73	-11	12.09	-1
1250	100	12.5	100	100	4.94	-9	1.8	-11	11.24	-2
1250	200	6.25	50	50	4.98	-9	1.74	-11	11.19	-2
1250	200	6.25	25	25	4.94	-9	1.72	-11	8.92	-1
1250	200	6.25	100	100	5.12	-9	1.74	-10	8.45	-2

Table 4.5: Summary of maximum incremental mobility and turn-on voltage for ZnO (~ 50 nm) and IGO (~ 50 nm) TFTs fabricated on themal silicon oxide and ZnO (~ 50 nm) TFT fabricating using ATO gate insulator for varying device dimensions.

4.2.4 Discussion

Contact resistance of ITO to ZnO and IGO channel layers and the effect of contact resistance on device performance are investigated and the results are presented in the previous sections of this chapter. This section discusses the extracted contact resistance data and explores possible explanations for the observed trends.

Dielectric	R_{SD}·W (with respect to R_{CH}·W)	ΔL (μm)
SiO_2	Indeterminate or Negligible	Negative or Positive
ATO	Indeterminate or Non-negligible	Positive

Table 4.6: Summary of contact resistance extractions for devices fabricated with SiO_2 and ATO gate insulators.

General trends observed for the contact resistance measurements are summarized in Table 4.6 for devices (transistor and TLM structures) fabricated using either SiO_2 or ATO as the gate insulator. Devices fabricated with thermal silicon oxide as the gate dielectric yield either an indeterminate or a negligible contact resistance with respect to the channel resistance and ΔL is found to be either positive or negative; while structures fabricated by employing ATO as the gate dielectric yield either an indeterminate or non-negligible contact resistance and a positive ΔL. Contact resistance and ΔL are reported here as indeterminate due to too much data variability.

A negative ΔL suggests that the effect channel length, L_{eff}, is larger than the drawn channel length. A larger effective channel length may be due to process variability such as over-etching and/or improper lift-off. Kanicki *et al*. suggest the possibility of an oxide layer existing at the contact, and thus effectively increasing the channel length [25]. Conversely, a positive ΔL, suggests that L_{eff} is smaller than the drawn length. A smaller effective channel length may arise from variations in processing, such as under-etching or improper lift-off.

The contact resistance extracted from ZnO/SiO_2 TFTs and ZnO/ATO TFTs is ~ 0 and 0.7-3 kΩ-cm, respectively. This difference in contact resistance may be the result of the differing dielectric layers, as is reported by Blanchet *et al*. who found a correlation between contact resistance and the organic dielectric material used as the gate insulator that may be the result of a chemical interaction at interface layers (i.e., dielectric/electrode and dielectric/semiconductor) [19]. As mentioned in Section 4.2.3, the difference in surface roughness between thermal silicon oxide and ATO may explain the difference in channel mobility. Surface roughness may also be a plausible explanation for the difference seen in contact resistance reported for devices employing SiO_2 and ATO as the gate insulators.

In summary, it is found that the measured resistance is not dominated by contact resistance effects. However, it is unclear whether the contact resistance is a negligible or a small effect due to the indeterminate nature of the data which is associated with data variability. Further work is required using smaller device dimensions in order to accurately assess the contact resistance of ITO to wide-band gap semiconductors such as ZnO and IGO, and to accurately observe the effects on contact resistance on device performance.

4.3 Conclusions

Determination of contact resistance of ITO to two wide-band gap semiconductors, ZnO and IGO, is attempted and the effects of contact resistance on device performance are investigated using transistor and TLM structures. Both thermal silicon oxide and ATO are employed as the gate insulator layer. It is observed that device performance does not degrade with the device dimensions used in this work. Devices fabricated with SiO_2 as the gate dielectric yield either an indeterminate or negligible contact resistance, and devices fabricated with an ATO gate insulator result in either an indeterminate or non-negligible contact resistance. A precise contact resistance could not be extracted due to the indeterminate nature of the data which is attributed to data variability. It is likely that a decrease in the channel length will decrease the data variation. Thus, further work with smaller device dimensions is required to accurately assess contact resistance of ITO on oxide-based channel layers.

5. STABILITY ASSESSMENT OF OXIDE-BASED THIN-FILM TRANSISTORS

This chapter focuses on implementation of the methodology developed in Chapter 3, Section 3.2.2 for assessing the stability of oxide-based TFTs. Device fabrication is also presented.

5.1 TFT fabrication

All devices used for this research are staggered, bottom-gate TFTs fabricated on 10 x 15 mm silicon substrates with thermally grown SiO_2. A cross-section and a plan view of a TFT are shown in Fig. 5.1. The gate dielectric is a 100 nm thick thermally grown SiO_2 on top of a p-type Si wafer. After SiO_2 is etched from the backside of the wafer, tantalum (Ta) and gold (Au) are deposited; Ta (10 nm) serves as an adhesion layer between the Au (300 nm) and silicon substrate. The substrates with thermal oxide and Au/Ta are supplied by the Hewlett-Packard Company. The Si/Ta/Au stack constitutes the gate contact.

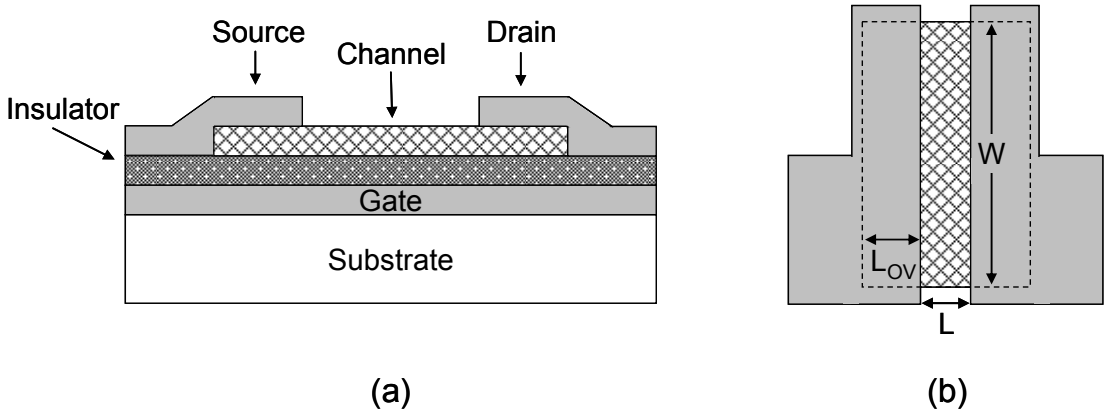

Figure 5.1: (a) Cross-section and (b) plan-view of a bottom-gate TFT, where L and W are the channel length and width, respectively.

The channel layers are deposited via RF magnetron sputtering using a 2 inch diameter ceramic target (Cerac, Inc.; ZnO, ZIO (1:1 molar ratio of $ZnO:In_2O_3$), and IGO (1:1 molar ratio of $In_2O_3:Ga_2O_3$)) in an Ar/O_2 ambient (90%/10%) at a pressure of 5 mTorr, power density of ~ 2.5 W/cm^2 for ZnO and ZIO and ~ 3.7 W/cm^2 for IGO, a target-to-substrate distance of ~ 10.2 cm, and with no intentional substrate heating. The channel layers are patterned via a shadow mask and are typically ~ 35–50 nm thick. The channel length and width are 200 and 1000 μm, respectively. After deposition of the semiconductor layer, the sample is furnace annealed in air at a temperature ranging from 200 to 800 °C. Lastly, ~ 200 nm of aluminum is evaporated and patterned via a shadow mask to form the source and drain contacts. The processing parameters for ZnO, ZIO, and IGO are tabulated in Table 5.1.

Channel Material	T_{Anneal} (°C)	Ambient (Ar/O_2)	Pressure (mTorr)	Power Density (W/cm^2)	Target-Substrate-Distance (cm)	Thickness (nm)
ZnO	200–600	90%/10%	5	~ 2.5	~ 10.2	~ 50
ZIO (1:1, $ZnO:In_2O_3$)	200–400	90%/10%	5	~ 2.5	~ 10.2	~ 35
IGO (1:1, $In_2O_3:Ga_2O_3$)	200–600	90%/10%	5	~ 3.7	~ 10.2	~ 50

Table 5.1: Summary of process parameters for TFTs fabricated on thermal silicon oxide and furnace annealed; W/L = 5 with L = 200 μm.

5.2 Electrical characterization

The trends in I_D, V_{ON}, mobility, and hysteresis are investigated for ZnO, ZIO, and IGO channel materials. To assess device stability as a function of temperature, TFTs for each channel material are annealed at temperatures in the range of 200 to 800 °C. The results are presented in the following sections.

5.2.1 ZnO TFTs

Figure 5.2 displays the drain current as a function of time for ZnO TFTs fabricated on thermal silicon oxide and furnace annealed at 200, 400, and 600 °C. Current is monitored over a time period of 10^5 s during which the gate and drain are each biased at 30 V. Drain current characteristics is also shown for ZnO TFT deposited via DC reactive sputtering [29] on spin-coat synthesized aluminum phosphate (AlPO) gate insulator [30], annealed at 600 °C and biased at V_{DS} = 30 V and V_{GS} = 40. Figure 5.2 show decreasing trends in I_D for TFTs annealed at 200, 400, and 600 °C with bias stress, while DC reactive sputtered ZnO TFT results in an increasing trend in I_D. These devices are discussed in detail in this section and Section 5.2.2.

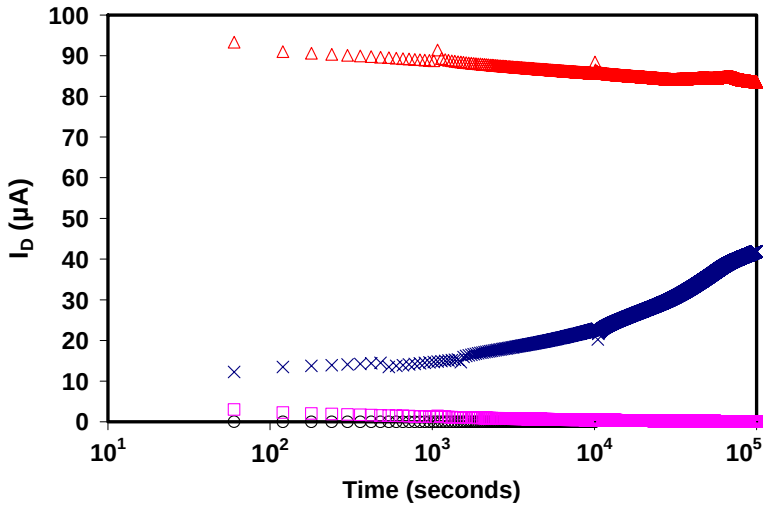

Figure 5.2: I_D–time plot for ZnO TFTs under bias stressing; V_{DS} = 30 V and V_{GS} = 30 V. The ZnO channel layers are ~ 50 nm thick, deposited on thermal silicon oxide, and furnace annealed in air at annealed at 200 (circles), 400 (squares), and 600 °C (triangles), respectively. Reactive sputtered ZnO TFT fabricated on spin coat synthesized AlPO annealed at 600 °C (x's) is biased at V_{DS} = 30 V and V_{GS} = 40 V. The channel length is 200 μm and the channel width is 1000 μm.

Figure 5.3 displays both the drain current (circles) and gate leakage current (x's) as a function of time for ZnO TFTs annealed at 200 (Fig. 5.2 (a)), 400 (Fig. 5.2 (b)), and 600 °C (Fig. 5.2 (c)). Current is monitored over a time period of 10^5 s (10^4 s for the TFT annealed at 200 °C) during which the gate and drain are each biased at 30 V. The bias stressing is interrupted at t = 10^3, 10^4, and 10^5 s at

which time a full characterization suite is performed, as described in Section 3.2.2. As depicted in Fig. 5.3(a) for the TFT annealed at 200 °C, the drain current shows a decreasing trend and a reduction from ~ 37 to ~ 0 nA after 10^3 s of stressing. Between t = 10^3 and 10^4 s, $I_D \approx I_G$, showing that the device is no longer in the "on" state. Figure 5.3(b), corresponding to the TFT annealed at 400 °C, also shows a decreasing trend and reduction from ~ 3 μA to ~ 60 nA after 10^5 s of stressing; I_G is on the order of 10^{-11} A. Figure 5.3(c), corresponding to the TFT annealed at 600 °C, illustrates a slight decreasing trend in the drain current after 10^5 s of stressing, reducing from ~ 90 to ~ 80 μA; I_G is on the order of 10^{-11}-10^{-12} A. The discontinuities seen at t = 10^3 and 10^4 s are artifacts created as a result of interrupting the constant-bias stressing to obtain the characterization suite data.

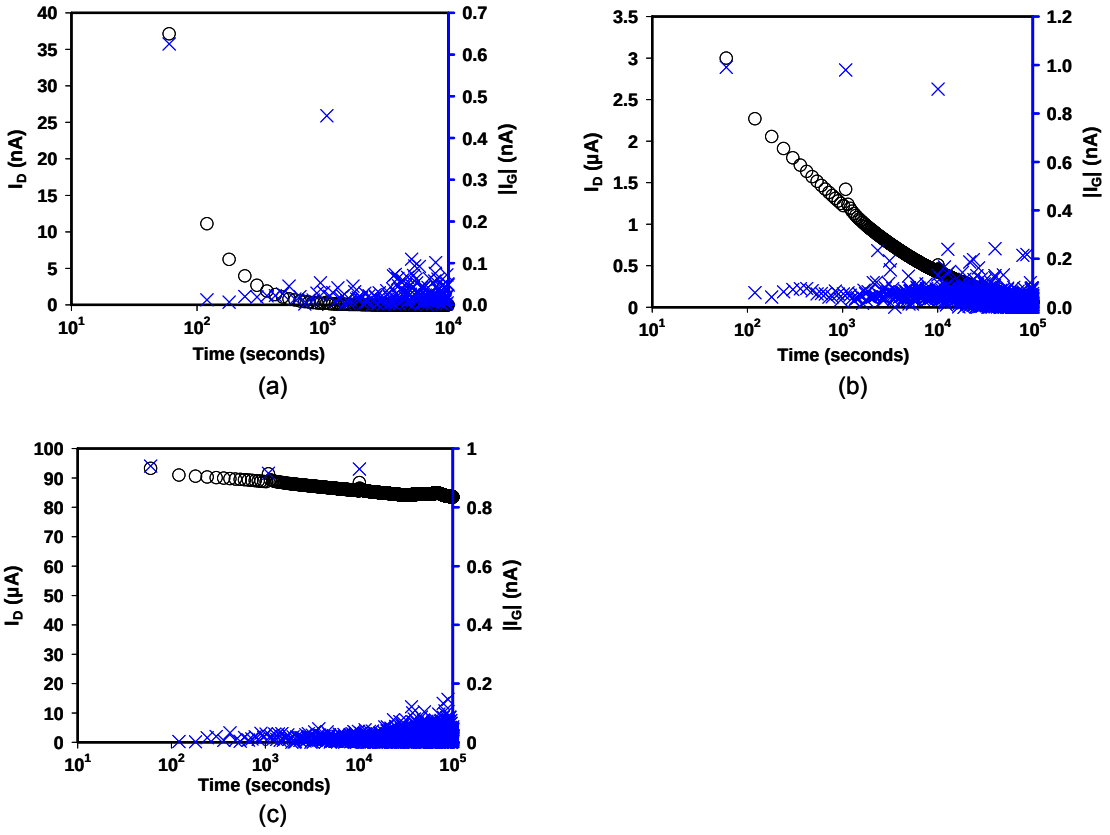

Figure 5.3: I_D–time (circles) plots for ZnO TFTs under constant bias stressing at $V_{DS} = V_{GS} = 30$ V. The ZnO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, and (c) 600 °C. The channel length and width are 200 and 1000 μm, respectively.

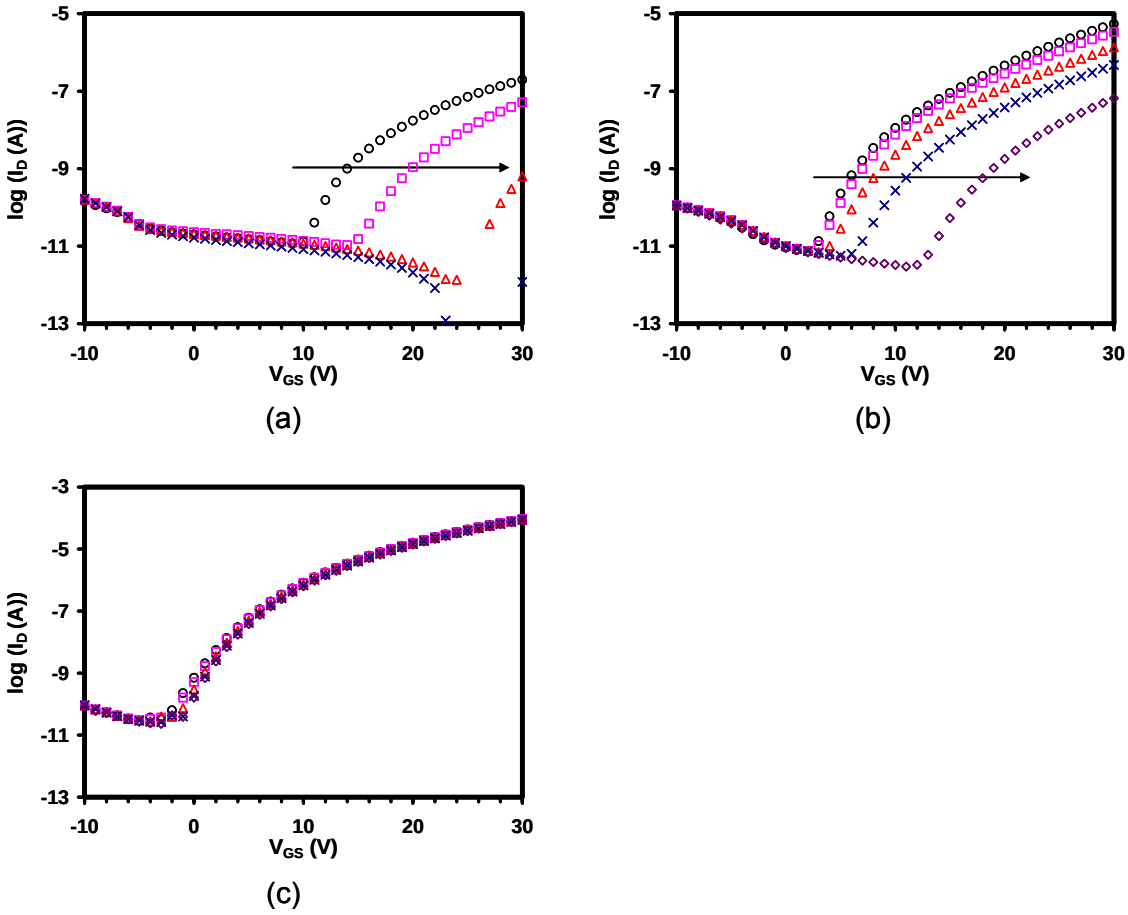

Figure 5.4: $\log(I_D)$–V_{GS} transfer curves for ZnO TFTs under constant bias stressing at $V_{DS} = V_{GS} = 30$ V. The ZnO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, and (c) 600 °C. The channel length and width are 200 and 1000 μm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

The drain current, plotted on a logarithmic scale, is shown as a function of gate voltage in Fig. 5.4. with the gate bias swept from -10 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 30 V. From Figs. 5.4(a) and (b), the turn-on voltage becomes more positive with stressing which results in a decrease in the drain current on-to-off ratio for ZnO TFTs annealed at 200 and 400 °C. From Fig 5.4, it is evident that the 200 and 400 °C anneal exhibit a positive shift in V_{ON} with increasing bias stress duration. A negligible change in V_{ON} is observed for the ZnO TFT annealed at 600 °C, as observed in the plot of $\log(I_D)$-V_{GS} in Fig. 5.3(c). V_{ON} and $I_{ON\text{-}OFF}$ are summarized for the different anneal temperatures in Tables 5.2-5.4.

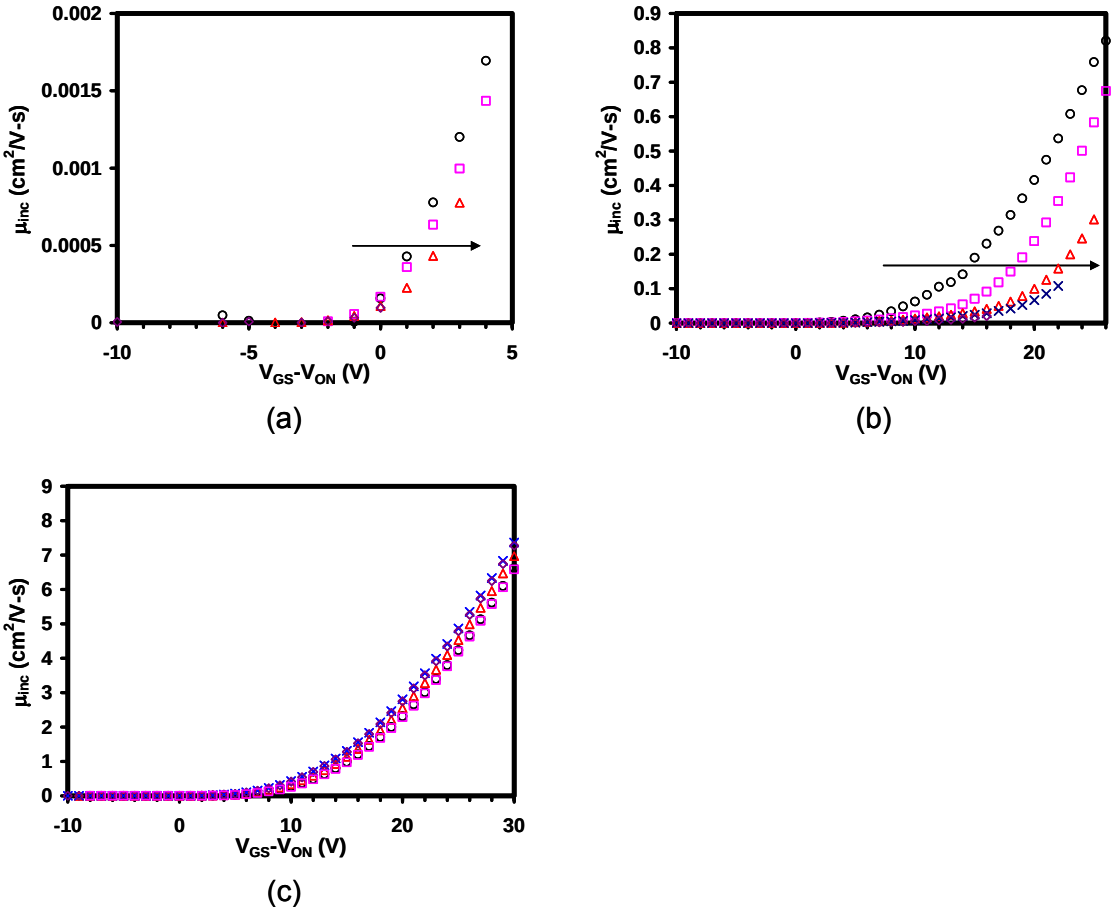

Figure 5.5: Incremental mobility-overvoltage curves for ZnO TFTs under constant bias stressing at V_{DS} = V_{GS} = 30 V. The ZnO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, and (c) 600 °C. The channel length and width are 200 and 1000 μm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

The incremental mobility is shown as a function of overvoltage in Fig. 5.5. The overvoltage, V_{OVER}, is the voltage applied beyond V_{ON}, i.e., $V_{OVER} = V_{GS} - V_{ON}$. Mobility data is extracted from a transfer curve of $\log(I_D)$-V_{GS} with V_{DS} = 1 V and with the gate swept from -10 V ≤ V_{GS} ≤ 30 V in 1 V steps. From Fig 5.5(b), it is evident that $\mu_{inc}(V_{GS})$ curves shift to the right (V_{ON} shift) and that μ_{inc} at a constant overvoltage decreases for TFTs annealed 200 and 400 °C. A negligible change in μ_{inc} is observed for ZnO TFT annealed at 600 °C. Incremental mobility extracted at V_{OVER} for the different anneal temperatures is summarized in Tables 5.2-5.4. Notice the overvoltage applied to each TFT

differs due to high turn-on voltages, i.e., 2 V for the TFT annealed at 200 °C, 16 and 20 V for the TFTs annealed at 400 and 600 °C, respectively. This is the result of unavailable data at large overvoltages.

Figure 5.6 is a transfer curve $\log(I_D)$-V_{GS} plot with V_{DS} = 1 V at time t = 0 s for a ZnO TFT annealed at 200 °C. This plot shows clockwise hysteresis characteristics with V_{ON} = 7 V and 11 V for the forward sweep and reverse sweep, respectively, resulting in a 4 V shift in the turn-on voltage in the positive direction. Hysteresis is most pronounced during the initial test (t = 0 s) in the characterization suite and is negligible for subsequent tests, thus indicating that the device is not initially stable, but requires a "burn-in" step. Tables 5.2-5.4 quantatively summarize hysteresis in terms of the change on V_{ON}.

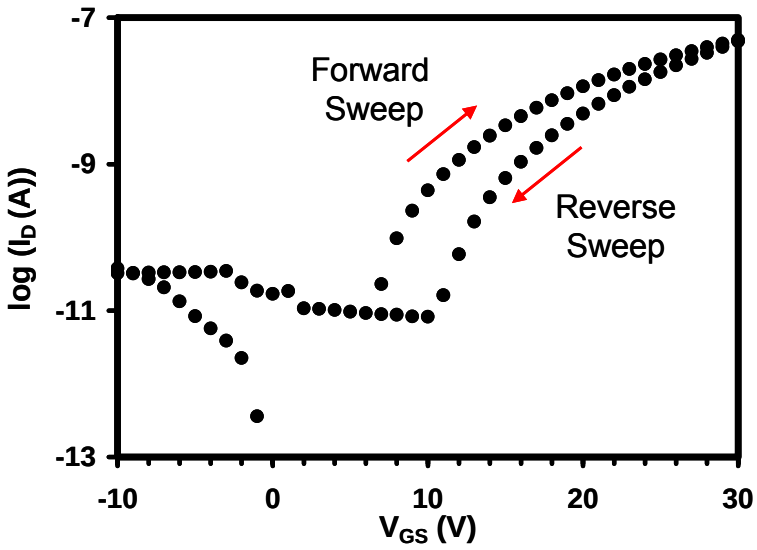

Figure 5.6: $\log(I_D)$-V_{GS} transfer curve with V_{DS} = 1 V showing clockwise hysteresis for a ZnO channel (~ 50 nm) TFT fabricated on thermal silicon oxide annealed at 200 °C is taken at t = 0 s. For the forward sweep, V_{ON} = 7 V, the reverse sweep gives V_{ON} = 11 V. The sweep rate is ~ 1V/s.

Stress Time (s)	V_{ON} (V)	$\mu_{inc}(V_{OVER} = 2\ V)$ (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=30 V, V_{GS}=30 V	Hysteresis (ΔV_{ON} (V))
0	10	0.0012	10^3	6.8×10^{-8}	+4
0^+	15	0.001	10^2	3.0×10^{-8}	+1
10^3	27	0.0008	10^1	4.0×10^{-10}	0
10^4	30	-	0	1.6×10^{-11}	0
Rest Time					
30 days	5	0.0009	10^3	2.3×10^{-7}	2

Table 5.2: Summary of bias stress measurement for a ZnO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 200 °C; W/L = 5 with L = 200 μm. The 30 day time entry refers to the recovery duration, while the other entries are for the stress times at $V_{DS} = V_{GS} = 30$ V.

Stress Time (s)	V_{ON} (V)	$\mu_{inc}(V_{OVER} = 16\ V)$ (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=30 V, V_{GS}=30 V	Hysteresis (ΔV_{ON} (V))
0	3	0.23	10^4	3.6×10^{-6}	0
0^+	3	0.09	10^4	2.8×10^{-6}	-1
10^3	4	0.04	10^3	1.3×10^{-6}	0
10^4	7	0.03	10^3	4.7×10^{-7}	0
10^5	14	0.02	10^2	6.6×10^{-8}	0
Rest Time					
30 days	3	0.22	10^4	3.4×10^{-6}	0

Table 5.3: Summary of bias stress measurement for ZnO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 400 °C; W/L = 5 with L = 200 μm. The 30 day time entry refers to the recovery duration, while the other entries are for the stress times at $V_{DS} = V_{GS} = 30$ V.

Stress Time (s)	V_{ON} (V)	$\mu_{inc}(V_{OVER} = 20\ V)$ (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=30 V, V_{GS}=30 V	Hysteresis (ΔV_{ON} (V))
0	-2	2.31	10^5	9.2 x 10^{-5}	0
0^+	-4	2.28	10^5	9.2 x 10^{-5}	0
10^3	-2	2.55	10^5	9.0 x 10^{-5}	0
10^4	0	2.81	10^5	8.7 x 10^{-5}	0
10^5	-2	2.75	10^5	8.5 x 10^{-5}	0
Rest Time					
30 days	-4	1.25	10^5	9.5 x 10^{-5}	0

Table 5.4: Summary of bias stress measurement for ZnO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 600 °C; W/L = 5 with L = 200 μm. The 30 day time entry refers to the recovery duration, while the other entries are for the stress times at $V_{DS} = V_{GS} = 30$ V.

A DUT is categorized as stable, relatively stable or unstable based on the data collected during constant-bias stress testing. If negligible changes in all the stability criteria, V_{ON}, I_D, and mobility, are observed over the course of testing, a TFT is considered to be stable. Otherwise the TFT is classified as unstable.

After bias stress testing, the DUT is allowed to rest for a period of approximately, 30 days for ZnO TFTs fabricated using SiO_2 as the gate insulator. This resting period allows the DUT to recover from the stress test measurement. After the recovery duration, a full characterization suite is performed on the DUT. The stability data collected from this measurement determines if the instabilities manifested during stress testing are reversible or irreversible with rest. For instabilities to be reversible, V_{ON}, I_D, and mobility, collected at time t = 0 s or 0^+ s are reproducible after a period of rest. If the values are not reproducible to within experimental error, the instabilities are considered to be irreversible with rest.

Bias stress measurements for ZnO TFTs annealed at 200, 400, 600 °C and are summarized in Tables 5.5. It is found that the higher temperature 600 °C anneal results in a stable device in comparison to TFTs annealed at 200 and 400 °C.

T_{Anneal} (°C)	ΔV_{ON}	$\Delta \mu_{inc}$	ΔI_D	After Rest	Stability
200	Positive	Decrease	Decrease	Irreversible	Unstable
400	Positive	Decrease	Decrease	Reversible	Unstable
600	Negligible	Negligible	Negligible	No change	Stable

Table 5.5: Summary of bias stress measurements for ZnO TFTs fabricated on thermal silicon oxide and furnace annealed in air; W/L = 5 with L = 200 μm.

5.2.2 Reactive sputtered ZnO TFT

In comparison to the ZnO TFTs discussed above, a ZnO TFT fabricated by DC reactive sputtering is investigated [29]. The channel layer is furnace annealed at 600 °C and deposited on top of a spin coat synthesized aluminum phosphate (AlPO) gate dielectric [30]. Current is monitored in Fig. 5.7(a) over a time period of $t = 10^5$ s during which the gate and drain are biased at 30 V and 40 V, respectively. The bias stressing is interrupted at $t = 10^3$, 10^4, and 10^5 s at which time a full characterization suite is performed. As depicted by Fig. 5.7(a), the drain current shows an increasing trend, I_D increases from ~ 12 to ~ 40 μA after 10^5 s of stressing; I_G is on the order of 10^{-11}-10^{-12} A.

The trend for V_{ON} is evident in the plot of $\log(I_D)$-V_{GS} in Fig. 5.7(b), where the gate bias is swept from $-20 \text{ V} \leq V_{GS} \leq 40 \text{ V}$ in 1 V steps with V_{DS} = 30 V. The turn-on voltage becomes more increases negatively with stressing, which results in the increase of the drain current on-to-off ratio; corresponding to $I_{ON\text{-}OFF} = 10^5$ for each sweep. V_{ON} and $I_{ON\text{-}OFF}$ are summarized in Table 5.6.

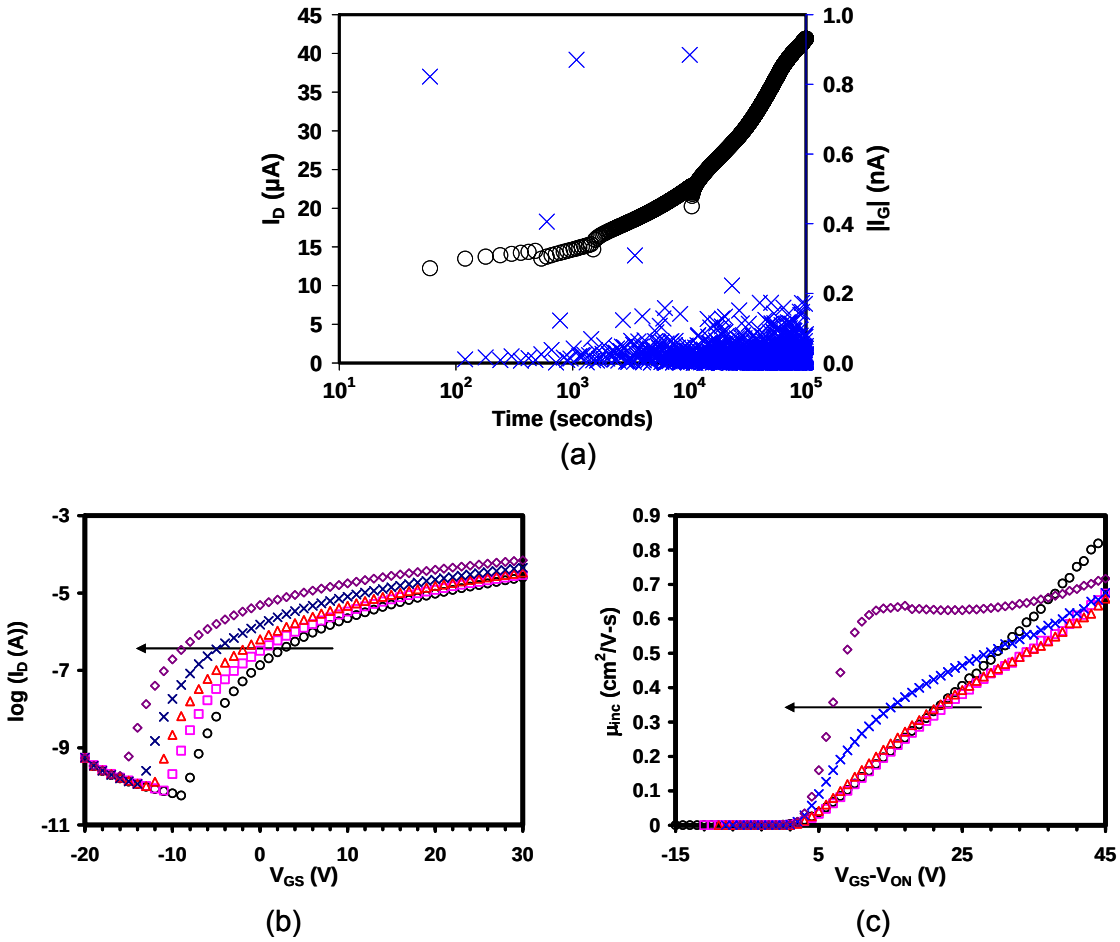

Figure 5.7: DC reactive sputtered ZnO channel (~ 50 nm) TFT fabricated on spin-coat synthesized AlPO annealed at 600 °C under constant bias stressing; V_{DS} = 30 V and V_{GS} = 40 V. (a) I_D–time plot, (b) log(I_D)–V_{GS} transfer curves, and (c) μ_{inc}(V_{GS}-V_{ON}) curves. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

The incremental mobility is shown as a function of gate voltage in Fig. 5.7(c). Mobility data is extracted from a transfer curve of log(I_D)-V_{GS} with V_{DS} = 1 V (Fig. 5.8). The gate is swept from -20 V ≤ V_{GS} ≤ 40 V in 1 V steps. As illustrated in Fig. 5.7(c), the curvature of μ_{inc}(V_{OVER}) is positive at t = 0 s, but becomes negative over the course of bias stressing. This curvature is particularly pronounced at the final stress time of 10^5 s. The maximum incremental mobility extracted at V_{over} = 20 V is summarized in Table 5.6.

Figure 5.8 is a transfer curve $\log(I_D)$-V_{GS} with V_{DS} = 1 V at time t = 0 s. This plot shows counter-clockwise hysteresis characteristics with V_{ON} = -4 V and -12 V for the forward sweep and reverse sweep, respectively, resulting in an 8 V shift in the turn-on voltage in the negative direction. Unlike all of the other devices discussed in this chapter, hysteresis is observed for all characterization sweeps.

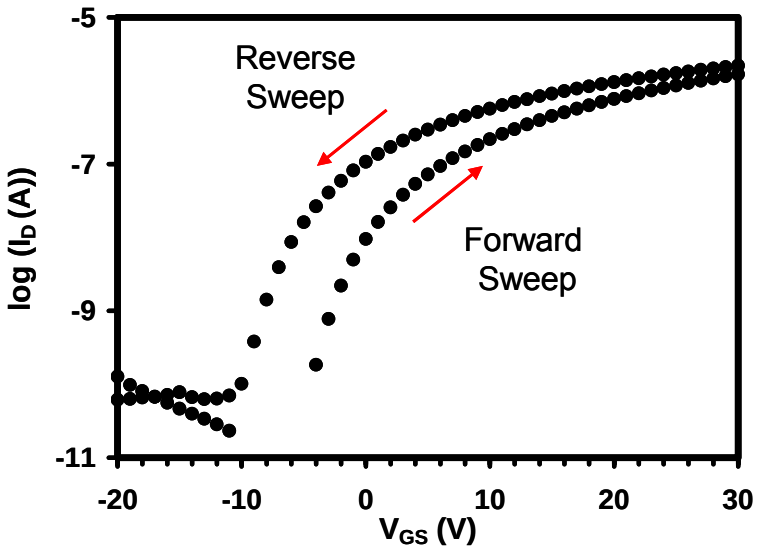

Figure 5.8: $\log(I_D)$-V_{GS} transfer curve with V_{DS} = 1 V showing counter-clockwise hysteresis for a DC reactive sputtered ZnO channel (~ 50 nm) TFT fabricated on spin-coat synthesized aluminum phosphate taken at t = 0 s. For the forward sweep, V_{ON} = -4 V, the reverse sweep gives V_{ON} = -12 V. The sweep rate is ~ 1V/s.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=30 V, V_{GS}=30 V	Hysteresis (ΔV_{ON} (V))
0	-8	0.31	10^5	2.9 x 10^{-5}	-8
0^+	-10	0.30	10^5	3.2 x 10^{-5}	-4
10^3	-12	0.32	10^5	3.6 x 10^{-5}	-3
10^4	-13	0.41	10^5	4.6 x 10^{-5}	-2
10^5	-15	0.63	10^5	7.0 x 10^{-5}	-2
Rest Time					
30 days	-18	0.33	10^5	5.5 x 10^{-5}	-5

Table 5.6: Summary of bias stress measurement for reactive sputtered ZnO (~ 50 nm) TFT fabricated on spin coat synthesized AlPO as the gate insulator and furrnace annealed in air at 600 °C; W/L = 5 with L = 200 μm. The 30 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = 30 and V_{GS} = 40 V.

Bias stress measurements of DC reactive sputtered ZnO on spin-coat synthesized AlPO are summarized in Table 5.7. After 30 days of rest, the DUT did not return to its original operating characteristics, indicating that the instabilities manifested during stressing are not reversible.

T_{Anneal} (°C)	ΔV_{ON}	$\Delta\mu_{inc}$	ΔI_D	After Rest	Stability
600	Negative	Increase	Increase	Irreversible	Unstable

Table 5.7: Summary of bias stress measurement for ZnO TFTs fabricated using spin-coat synthesized AlPO furnace annealed in air; W/L = 5 with L = 200 μm.

5.2.3 ZIO TFTs

Figure 5.9 displays the drain current as a function of time for ZIO TFTs fabricated on thermal silicon oxide and furnace annealed at 200 and 400 °C. Current is monitored over a time period of 10^5 s during which the gate and drain are each biased at 30 V. Figure 5.9 shows a decreasing trend in I_D for the TFT annealed at 200 °C, while the 400 °C anneal results in a negligible change. These devices are discussed in detail in this section.

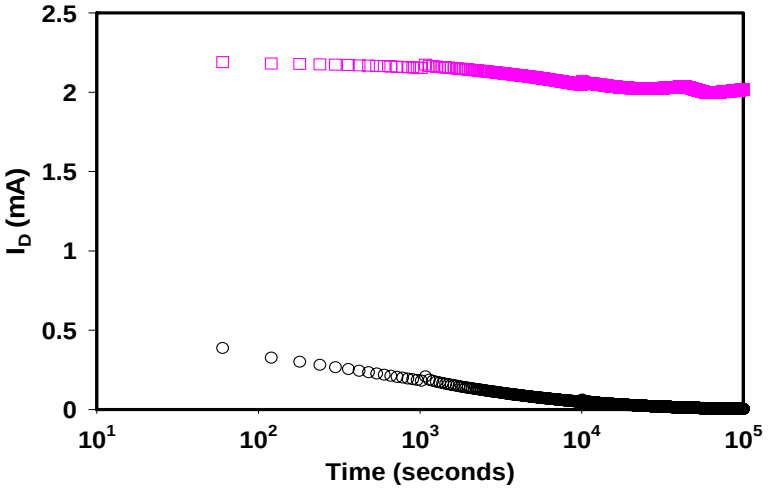

Figure 5.9: I_D–time plot for ZIO TFTs under bias stressing; V_{DS} = 30 V and V_{GS} = 30 V. The ZIO channel layers are ~ 35 nm thick, deposited on thermal silicon oxide, and furnace annealed in air at annealed at 200 (circles) and 400 °C (squares). The channel length and width are 200 and 1000 μm, respectively.

Figure 5.10 displays both the drain current (circles) and gate leakage current (x's) as a function of time for a ZIO TFT annealed at 200 °C (Fig. 5.10(a)) and 400 °C (Fig. 5.10(b)). Current is monitored over a time period of 10^5 s during which the gate and drain are each biased at 30 V. The bias stressing is interrupted at t = 10^3, 10^4, and 10^5 s at which time a full characterization suite is performed. As depicted in Fig. 5.10(a), the drain current shows a decreasing trend and a reduction from ~ 400 to ~ 4 μA after 10^5 s of stressing; I_G is on the order of 10^{-11}-10^{-12} A. Figure 5.10(b) also shows a negligible decrease after 10^5 s of stressing; I_G is on the order of 10^{-10} A.

The turn-on voltage is shown as a function of gate voltage in Fig. 5.11, where the gate bias is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps with V_{DS} = 30 V. V_{ON} increases positively with stressing, which results in the decrease of the drain current on-to-off ratio. Figure 5.11(b) exhibits negligible change in V_{ON} for ZIO TFT annealed at 400 °C. V_{ON} and I_{ON-OFF} are summarized for the different anneal temperatures in Tables 5.8-5.9.

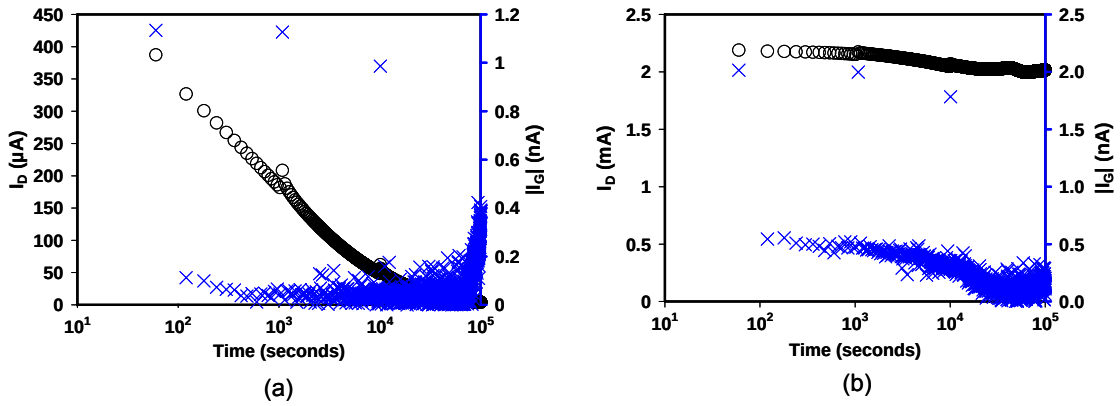

Figure 5.10: I_D–time (circles) plots for ZIO TFTs under constant bias stressing at V_{DS} = 30 V and V_{GS} = 30 V. The ZIO channel layer is ~ 35 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200 and (b) 400 °C The channel length and width are 200 and 1000 μm, respectively.

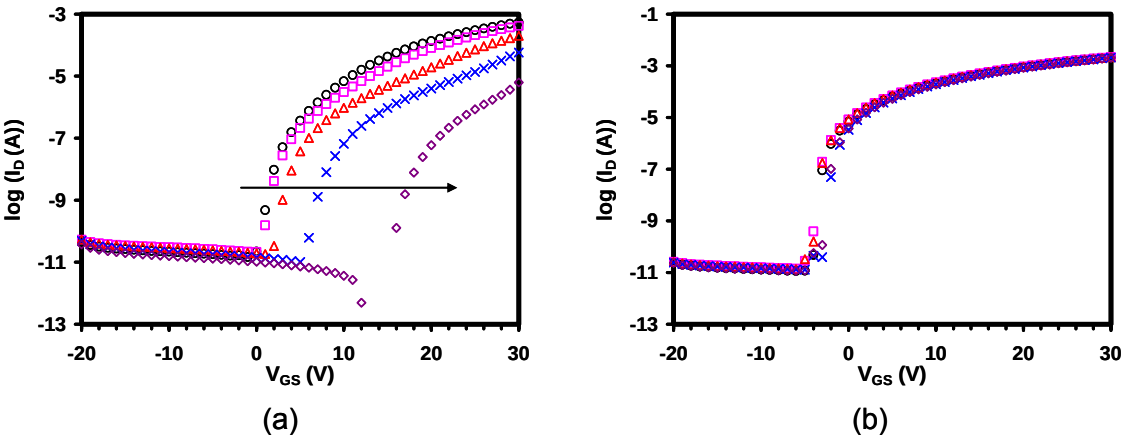

Figure 5.11: log(I_D)–V_{GS} transfer curves for ZIO TFTs under constant bias stressing at V_{DS} = 30 V and V_{GS} = 30 V. The ZIO channel layer is ~ 35 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200 °C and (b) 400 °C The channel length and width are 200 and 1000 μm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

The incremental mobility is shown as a function of over voltage in Fig. 5.12. Mobility data in Fig. 5.12(a) is extracted from a transfer curve of log(I_D)-V_{GS} with V_{DS} = 1 V (Fig. 5.13) for a ZIO TFT annealed at 200 °C. The gate is swept from -20 V ≤ V_{GS} ≤ 30 V in 1 V steps. The incremental mobility, extracted at V_{OVER} = 14 V, The mobility is tabulated in Table 5.8. With the exception of the mobility at t = 10^5 s, a decrease in the incremental mobility is observed. As illustrated in Fig. 5.12(a), the curvature

of μ_{inc} is initially (t = 0 s) negative, but becomes positive after t = 0^+ s. Negligible change in incremental mobility is observed for a ZIO TFT annealed at 400 °C, as shown in Fig. 5.12(b). The incremental mobility is extracted at V_{OVER} = 20 V and summarized for the different anneal temperatures in Tables 5.8-5.9

Figure 5.13 is a transfer curve log(I_D)-V_{GS} with V_{DS} = 1 V at time t = 0 s for a ZIO TFT annealed at 200 °C. This plot shows clockwise hysteresis characteristics with V_{ON} = -1 V and 1 V for the forward sweep and reverse sweep, respectively, resulting in n 2 V shift in the turn-on voltage in the positive direction. Hysteresis is most pronounced during the initial characterization sweep (t = 0 s) and is negligible for subsequent tests, thus indicating that the device is not initially stable, but requires a "burn-in" step.

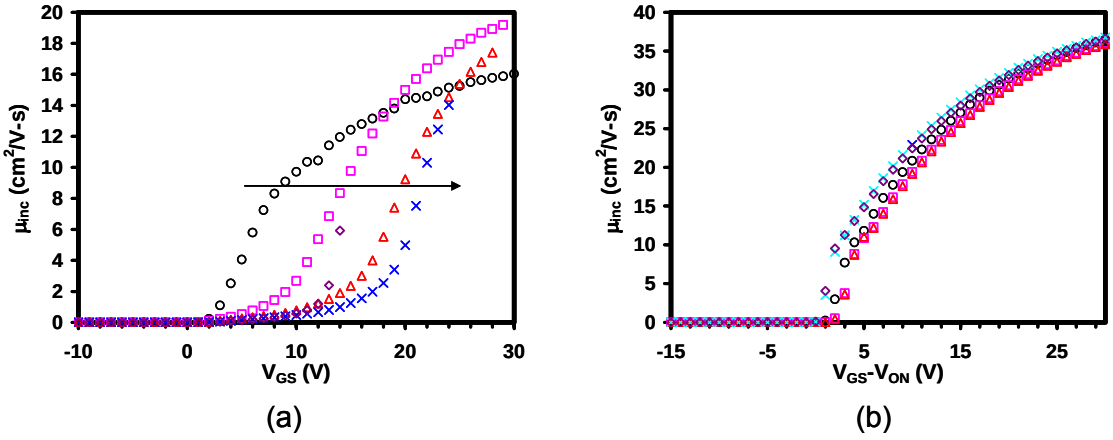

Figure 5.12: μ_{inc}–V_{GS}-V_{ON} curves for ZIO TFTs under constant bias stressing at V_{DS} = 30 V and V_{GS} = 30 V. The ZIO channel layer is ~ 35 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200 and (b) 400 °C The channel length and width are 200 and 1000 μm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

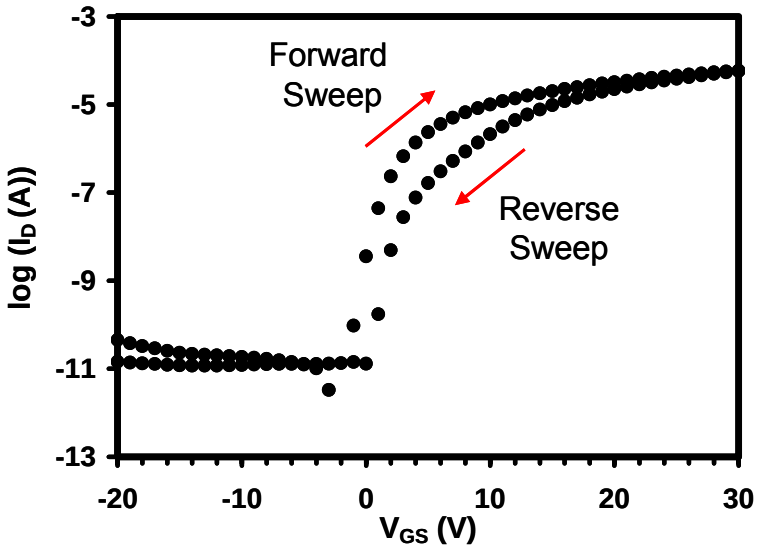

Figure 5.13: $\log(I_D)$-V_{GS} transfer curve showing clockwise hysteresis for a ZIO channel (~ 50 nm) TFT fabricated on thermal silicon oxide annealed at 200 C collected at t = 0 s. For the forward sweep, V_{ON} = -1 V, the reverse sweep gives V_{ON} = 1 V. The sweep rate is ~ 1V/s.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=30 V, V_{GS}=30 V	Hysteresis (ΔV_{ON} (V))
0	0	11.95	10^6	4.5×10^{-4}	+2
0^+	1	8.33	10^6	3.8×10^{-4}	0
10^3	2	1.89	10^6	2.0×10^{-4}	0
10^4	6	0.99	10^5	5.9×10^{-5}	0
10^5	16	5.92	10^4	6.5×10^{-6}	0
Rest Time					
13 days	2	13.01	10^6	5.4×10^{-4}	+2

Table 5.8: Summary of bias stress measurement for ZIO (~ 35 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 200 °C; W/L = 5 with L = 200 µm. The 13 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=25 V, V_{GS}=25 V	Hysteresis (ΔV_{ON} (V))
0	-5	31.45	10^6	2.2 x 10^{-3}	-1
0^+	-5	30.57	10^6	2.2 x 10^{-3}	0
10^3	-5	30.37	10^6	2.2 x 10^{-3}	0
10^4	-2	32.20	10^6	2.1 x 10^{-3}	-1
10^5	-5	31.89	10^6	2.0 x 10^{-3}	-1
Rest Time					
13 days	-1	33.05	10^6	2.0 x 10^{-3}	0

Table 5.9: Summary of bias stress measurement for ZIO (~ 35 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 400 °C; W/L = 5 with L = 200 μm. The 13 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Bias stress measurements for ZIO TFTs annealed at 200 and 400 °C are summarized in Table 5.10. The DUTs are allowed to rest for the duration of 13 days, however, the stability criteria for the ZIO TFT annealed at 200 °C did not return to its original operating characteristics, indicating that the instabilities manifested during stressing are not reversible. The 400 C annealed TFT results in a stable device.

T_{Anneal} (°C)	ΔV_{ON}	$\Delta\mu_{inc}$	ΔI_D	After Rest	Stability
200	Positive	Decrease	Decrease	Irreversible	Unstable
400	Negligible	Negligible	Negligible	No change	Stable

Table 5.10: Summary of bias stress measurement for ZIO TFTs fabricated on thermal silicon oxide and annealed in air; W/L = 5 with L = 200 μm.

5.2.3 IGO TFTs

Figure 5.14 displays the drain current as a function of time for IGO TFTs fabricated on thermal silicon oxide and furnace annealed at 200, 400, 600, and 800 °C. Current is monitored over a time period of 10^5 s during which the gate and drain are each biased at 25 V. TFTs with 200 and 400 °C observed a reduction in I_D after stressing. Higher temperature anneals show negligible change in I_D for 600 and 800 °C, respectively. These devices are discussed in detail in this section.

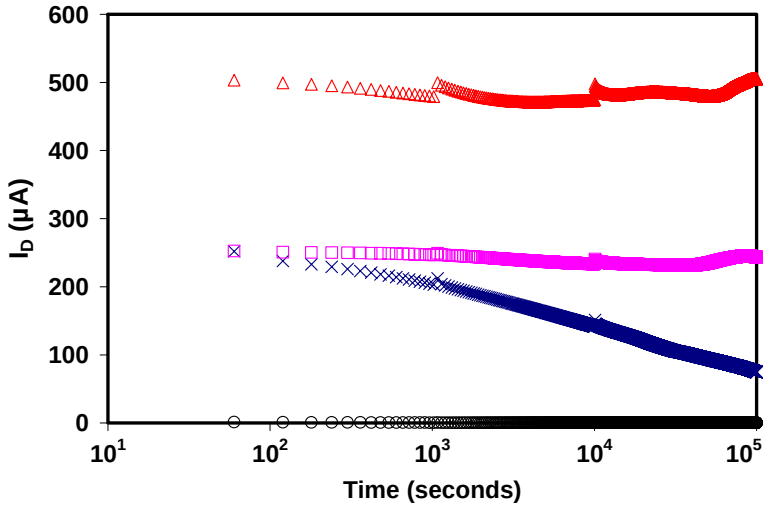

Figure 5.14: I_D–time plot for IGO TFTs under bias stressing; V_{DS} = 25 V and V_{GS} = 25 V. The IGO channel layers are ~ 50 nm thick, deposited on thermal silicon oxide, and furnace annealed in air at annealed at 200 (circles), 400 (x's), 600 (triangles), and 800 °C (squares), respectively. The channel length is 200 μm and the channel width is 1000 μm.

Figure 5.15 displays both the drain current (circles) and gate leakage current (x's) as a function of time for a IGO TFT annealed at 200 (Fig. 5.14(a)), 400 (Fig. 5.14(b)), 600 (Fig. 5.14(c)), and 800 °C (Fig. 5.14(d)). Current is monitored over a time period of 10^5 s during which the gate and drain are each biased at 25 V. The bias stressing is interrupted at t = 10^3, 10^4, and 10^5 s at which time a full characterization suite is performed, as described in Section 3.2.2. As depicted by Fig. 5.15(a), the drain current shows a decreasing trend and a reduction from ~ 1 μA to ~ 4 nA after 10^5 s of stressing; I_G is on the order of 10^{-11} A. The 400 °C anneal also exhibits a decreasing trend in the drain current, illustrated by Fig. 5.15(b), reducing from ~ 250 to ~ 75 μA after 10^5 s of stressing; I_G is on the order of 10^{-11}-10^{-12} A. Slight fluctuations are observed in the drain current for both the 600 and 800 °C anneals. Figure 5.15(c) shows I_D averaging at ~ 500 μA during the 10^5 s of stressing; I_G is on the order of 10^{-11} A. I_D averages to ~ 240 μA during the 10^5 s of stressing; I_G is on the order of 10^{-11}-10^{-12} A for the 800 °C anneal shown in Fig. 5.15(d).

The turn-on voltage is shown as a function of gate voltage in Fig. 5.16. For IGO TFTs annealed at 200, 400, 600, and 800 °C. For 200 and 400 °C anneals, the turn-on voltage becomes more positive with stressing which results in the decrease of the drain current on-to-off ratio. This trend in V_{ON} is evident in the plot of $\log(I_D)$-V_{GS} in Fig. 5.16(a), where the gate bias is swept from -20 V ≤ V_{GS} ≤ 25 V in 1 V steps with V_{DS} = 25 V. The turn-on voltage increases positive with stressing, which results in the decrease of the drain current on-to-off ratio. Negligible change in V_{ON} is observed for the higher temperature anneals of 600 and 800 °C. V_{ON} and I_{ON-OFF} are summarized for the different anneal temperatures in Tables 5.11-5.14.

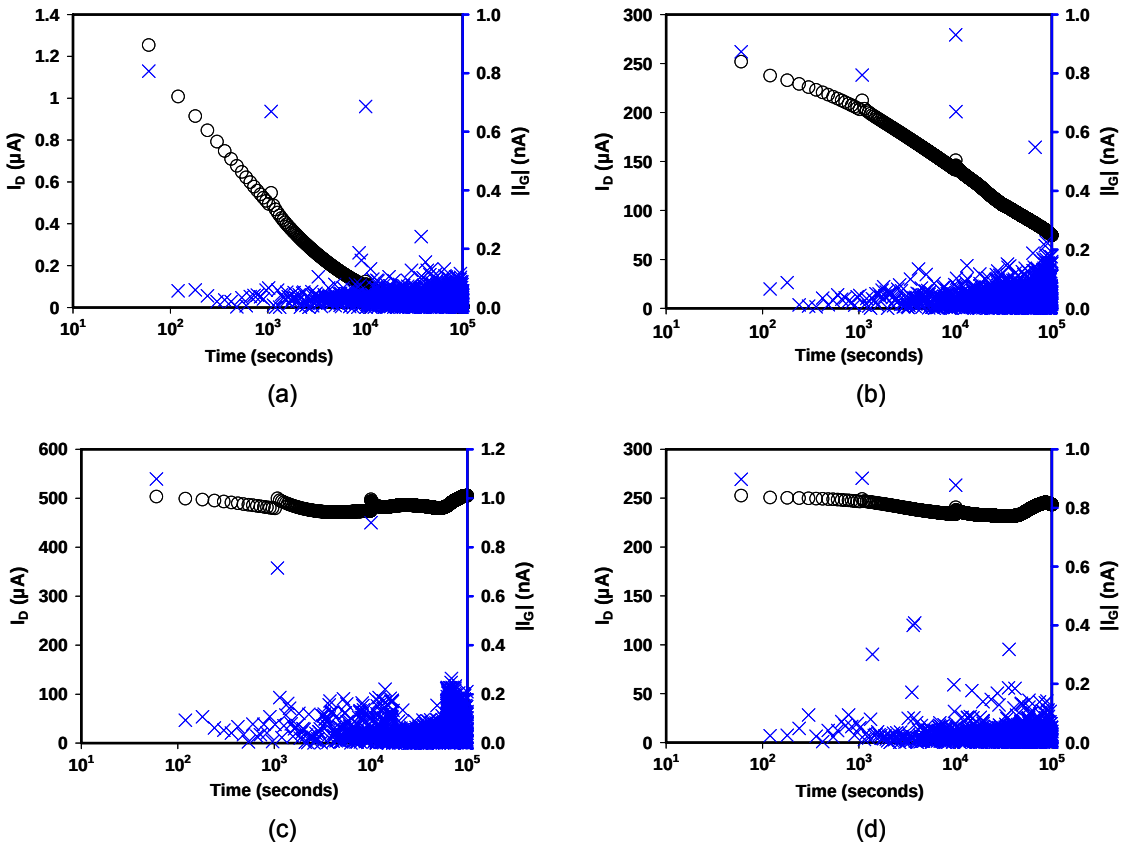

Figure 5.15: I_D-time (circles) plots for IGO TFTs under constant bias stressing at V_{DS} = 25 V and V_{GS} = 25 V. The IGO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, (c) 600, and (d) 800 °C. The channel length and width are 200 and 1000 μm, respectively.

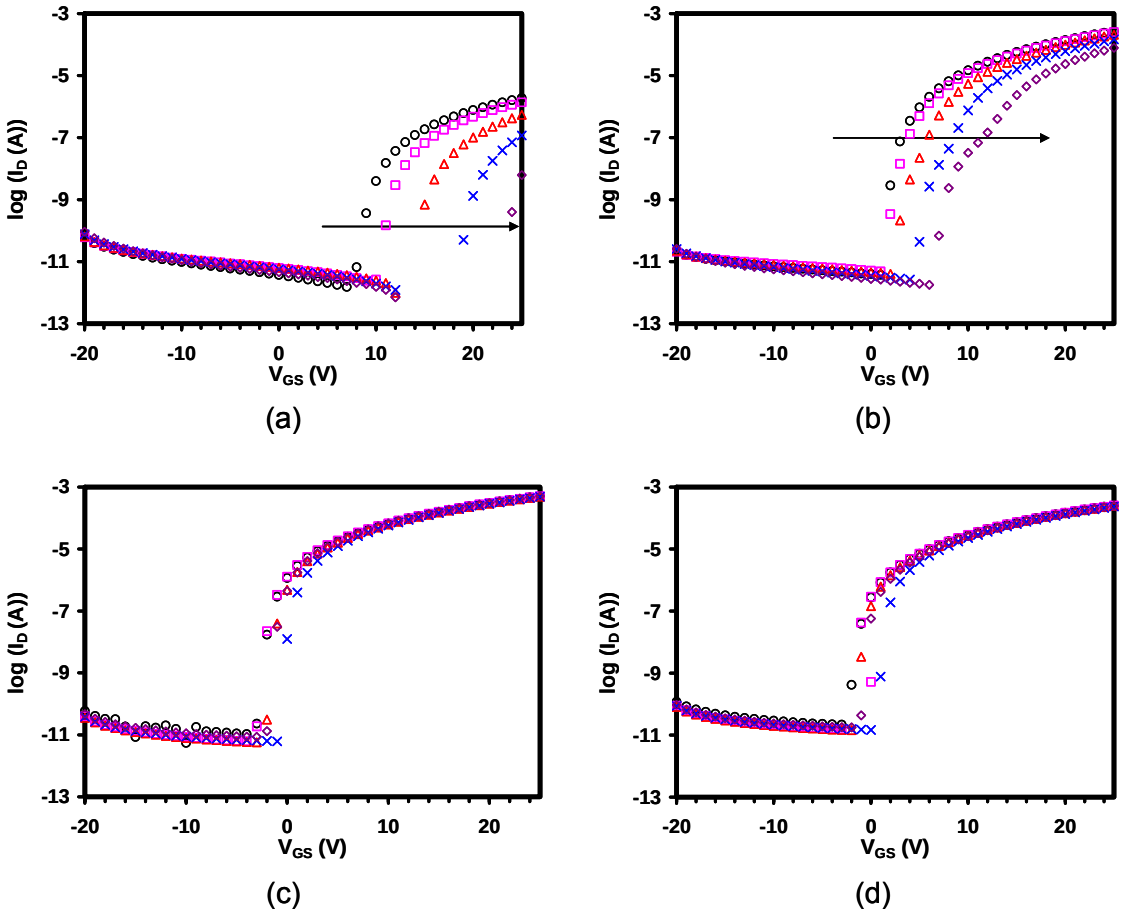

Figure 5.16: $\log(I_D)$–V_{GS} transfer curves for IGO TFTs under constant bias stressing at V_{DS} = 25 V and V_{GS} = 25 V. The IGO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, (c) 600, and (d) 800 °C. The channel length and width are 200 and 1000 µm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

The incremental mobility is shown as a function of overvoltage in Fig. 5.17. Mobility data in Fig. 5.17(a) is extracted from a transfer curve of $\log(I_D)$-V_{GS} with V_{DS} = 1 V (Fig. 5.18) for a IGO TFT annealed at 200 °C. The gate is swept from -20 V ≤ V_{GS} ≤ 25 V in 1 V steps. The incremental mobility is extracted at V_{OVER} = 4 V and summarized in Table 5.11. A decrease in incremental mobility, extracted at V_{OVER} = 17 is evident fro an IGO TFT annealed at 400 °C, as shown in Fig. 5.16(b). Negligible change in μ_{inc} is observed for IGO TFTs annealed at 600 and 800 °C, as evident in the plots of $\log(I_D)$-V_{GS} in Fig. 5.17(c) and (d). Incremental mobility as a function of overvoltage is summarized for the different anneal temperatures in Tables 5.11-5.14.

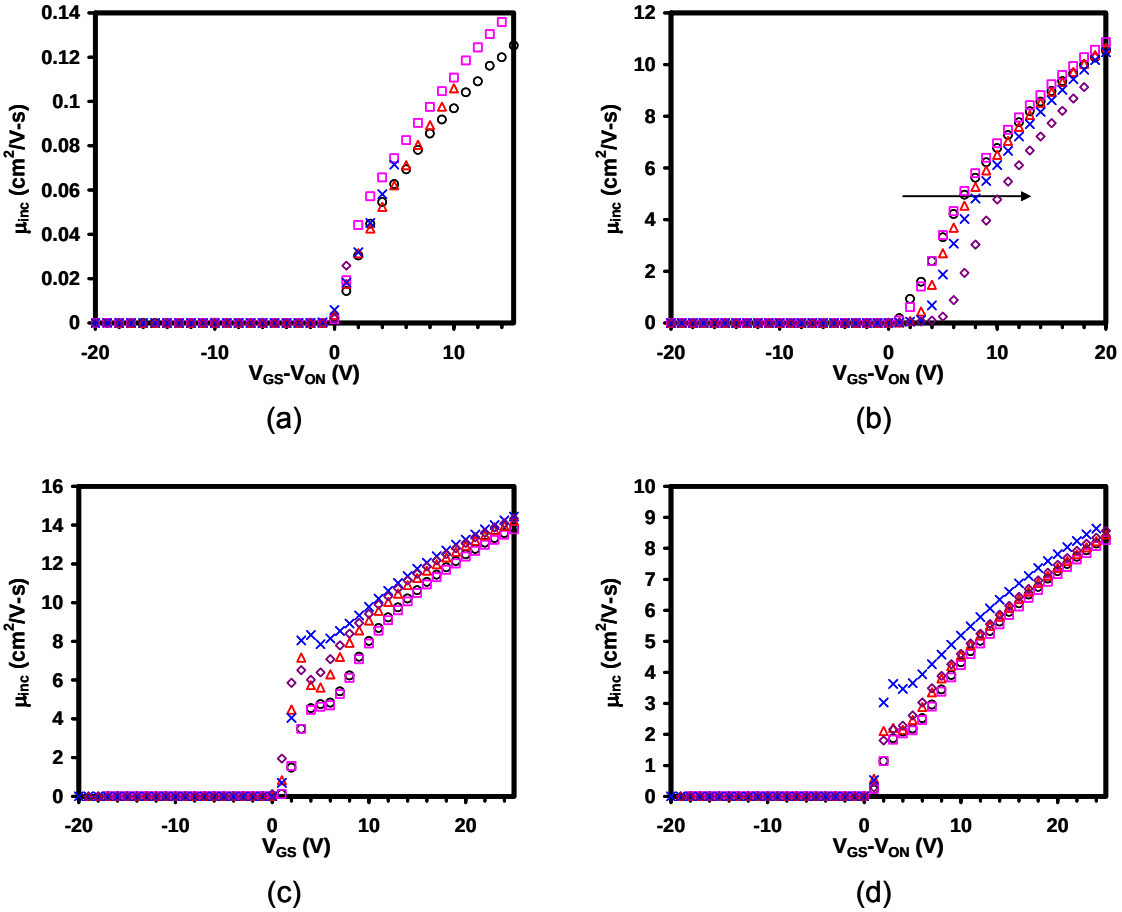

Figure 5.17: Incremental mobility-overvoltage curves for IGO TFTs under constant bias stressing at V_{DS} = 25 V and V_{GS} = 25 V. The IGO channel layer is ~ 50 nm thick, deposited via RF sputtering on thermal silicon oxide and furnace annealed at (a) 200, (b) 400, (c) 600, and (d) 800 °C. The channel length and width are 200 and 1000 μm, respectively. The arrow indicates the direction of increasing bias stress duration for stress times of 0 (circles), 0^+ (squares), 10^3 (triangles), 10^4 (x's), and 10^5 s (diamonds).

Figure 5.18 is a transfer curve $\log(I_D)$-V_{GS} with V_{DS} = 1 V for an IGO TFT annealed at 200 °C, collected at time t = 0 s. This plot shows clockwise hysteresis characteristics with V_{ON} = 7 V and 9 V for the forward sweep and reverse sweep, respectively, resulting in a 2 V shift in the turn-on voltage in the positive direction. Hysteresis is most pronounced during the initial characterization sweep and negligible for subsequent tests, thus indicating that the device is not initially stable, but requires a "burn-in" step.

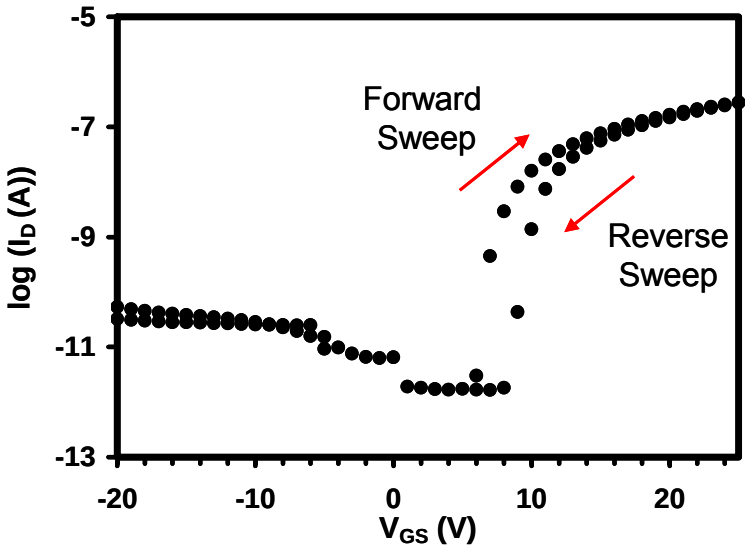

Figure 5.18: $\log(I_D)$-V_{GS} transfer curve showing clock-wise hysteresis for a IGO channel (~ 50 nm) TFT fabricated on thermal silicon oxide taken at t = 0 s. For the forward sweep, V_{ON} = 7 V, the reverse sweep gives V_{ON} = 9 V. The sweep rate is ~ 1V/s.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=25 V, V_{GS}=25 V	Hysteresis (ΔV_{ON} (V))
0	10	0.05	10^4	1.4 x 10^{-6}	+2
0^+	11	0.07	10^3	1.2 x 10^{-6}	0
10^3	15	0.05	10^3	5.2 x 10^{-7}	0
10^4	20	0.06	10^2	1.2 x 10^{-7}	0
10^5	24	-	10^2	6.3 x 10^{-9}	0
Rest Time					
52 days	7	0.06	10^3	2.0 x 10^{-6}	+3

Table 5.11: Summary of bias stress measurement for IGO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 200 °C; W/L = 5 with L = 200 µm. The 52 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=25 V, V_{GS}=25 V	Hysteresis (ΔV_{ON} (V))
0	2	9.66	10^6	2.5 x 10^{-4}	0
0^+	2	9.94	10^6	2.4 x 10^{-4}	0
10^3	3	9.71	10^6	2.1 x 10^{-4}	0
10^4	6	9.43	10^6	1.5 x 10^{-4}	0
10^5	7	8.69	10^5	7.9 x 10^{-5}*	0
Rest Time					
52 days	2	8.23	10^6	2.0 x 10^{-4}	+1

* I_D from I_D-V_{DS} taken at V_{DS} = 20 V, V_{GS} = 25 V.

Table 5.12: Summary of bias stress measurement for IGO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 400 °C; W/L = 5 with L = 200 μm. The 52 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=25 V, V_{GS}=25 V	Hysteresis (ΔV_{ON} (V))
0	-2	12.49	10^6	5.0 x 10^{-4}	0
0^+	-2	12.37	10^6	5.0 x 10^{-4}	0
10^3	-1	12.94	10^6	5.0 x 10^{-4}	0
10^4	0	13.25	10^6	5.0 x 10^{-4}	0
10^5	-1	13.08	10^6	5.1 x 10^{-4}	0
Rest Time					
52 days	-3	12.71	10^6	5.4 x 10^{-4}	0

Table 5.13: Summary of bias stress measurement for IGO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 600 °C; W/L = 5 with L = 200 μm. The 52 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Stress Time (s)	V_{ON} (V)	μ_{inc} (cm^2/V-s)	I_{ON-OFF}	I_D (A) from I_D-V_{DS} @ V_{DS}=25 V, V_{GS}=25 V	Hysteresis (ΔV_{ON} (V))
0	-2	7.26	10^6	2.5 x 10^{-4}	-1
0^+	-2	7.16	10^6	2.5 x 10^{-4}	-1
10^3	-1	7.37	10^6	2.5 x 10^{-4}	0
10^4	1	7.81	10^6	2.4 x 10^{-4}	+1
10^5	-1	7.46	10^6	2.5 x 10^{-4}	0
Rest Time					
52 days	-3	7.20	10^6	2.7 x 10^{-4}	0

Table 5.14: Summary of bias stress measurement for IGO (~ 50 nm) TFT fabricated on thermal silicon oxide and furnace annealed in air at 800 °C; W/L = 5 with L = 200 μm. The 52 day time entry refers to the recovery duration, while the other entries are for the stress times at V_{DS} = V_{GS} = 30 V.

Bias stress measurements for IGO TFTs annealed at 200, 400, 600, and 800 °C and are summarized in Table 5.15. After a resting period of 52 days, it is found that the IGO TFT annealed at 200 °C did not return to its original operating characteristics, indicating that the instabilities manifested during stressing are not reversible. Similar to ZnO, IGO devices are stable at higher temperature anneals, 600 and 800 °C.

T_{Anneal} (°C)	ΔV_{ON}	$\Delta\mu_{inc}$	ΔI_D	After Rest	Stability
200	Positive	Negligible	Decrease	Irreversible	Unstable
400	Positive	Decrease	Decrease	Reversible	Unstable
600	Negligible	Negligible	Negligible	No Change	Stable
600^2	Negligible	Negligible	Negligible	No Change	Stable

Table 5.15: Summary of bias stress measurement for IGO TFTs fabricated on thermal silicon oxide and annealed in air; W/L = 5 with L = 200 μm.

5.2.4 Discussion

The methodology proposed for assessing the stability of oxide-based channel materials and the results of devices tested using this method are presented in the previous sections of this chapter. This section summarizes trends in the predetermined stability criteria, ΔI_D, ΔV_{ON}, and $\Delta \mu_{inc}$, gathered for ZnO, ZIO, and IGO and explores the possible mechanisms behind instabilities manifested during bias stressing.

Channel Material	T_{Anneal} (°C)	ΔV_{ON}	$\Delta \mu_{inc}$	ΔI_D	Hysteresis	After Rest	Stability
ZnO	200	Positive	Decrease	Decrease	Clockwise[1]	Irreversible	Unstable
ZnO	400	Positive	Decrease	Decrease	No	Reversible	Unstable
ZnO	600	Negligible	Negligible	Negligible	No	No Change	Stable
ZnO[2]	600	Negative	Increase	Increase	Counter-clockwise	Irreversible	Unstable
ZIO	200	Positive	Decrease	Decrease	Clockwise[1]	Irreversible	Unstable
ZIO	400	Negligible	Negligible	Negligible	No	No Change	Stable
IGO	200	Positive	Negligible	Decrease	Clockwise[1]	Irreversible	Unstable
IGO	400	Positive	Decrease	Decrease	No	Reversible	Unstable
IGO	600	Negligible	Negligible	Negligible	No	No Change	Stable
IGO	800	Negligible	Negligible	Negligible	No	No Change	Stable

[1] Hysteresis is typically observed, if at all, only during the initial characterization sweep (t = 0 s) and is then found to be negligible for subsequent sweeps.
[2] ZnO channel deposited via reactive sputtering on spin coat synthesized AlPO gate insulator.

Table 5.16: Summary of bias stress measurements for TFTs fabricated with ZnO, ZIO, and IGO channel materials and a thermal silicon oxide gate insulator (except where noted), and furnace annealed at temperatures in the range of 200 to 800 °C; W/L = 5 with L = 200 μm.

Bias stress measurements are summarized in Table 5.16 for wide-band gap TFTs annealed at temperatures ranging from 200 to 800 °C. Stress measurements reveal that higher anneal temperatures are needed to fabricate stable devices. Data obtained for ZnO TFTs fabricated on SiO_2 and annealed at 200 and 400 °C show an increasing positive shift for V_{ON} and a decrease in mobility and I_D. Negligible changes in all parameters are observed for the ZnO TFT annealed at 600 °C. From this trend one might expect an 800 °C anneal for a ZnO TFT to result in a stable device. However, ZnO fully crystallizes at 800 °C (ZnO is poly-crystalline as-deposited) so that these 800 °C annealed devices have immeasurable

low currents. The reactively sputtered ZnO TFT fabricated using spin coat synthesized AlPO annealed at 600 °C results in a negative shift in V_{ON} and increasing trends in both mobility and drain current. It should be noted that the reactively sputtered ZnO on AlPO TFt\T is presented in order to show an example of a negative shift in V_{ON}, a positive increase in I_D, and of counter-clockwise hysteresis. ZIO TFTs annealed at 200 °C show an increasing positive shift for V_{ON} and decrease in mobility and I_D, while negligible changes in all parameters are observed for the ZIO TFT annealed at 400 °C. ZIO TFTs annealed at 600 and 800 °C exhibit extremely negative turn-on voltages (> -50 V); therefore, device stability for these devices is not investigated. IGO TFTs exhibit similar results to ZnO TFTs (fabricated on thermal silicon oxide as the gate insulator) in that lower temperature anneals, 200 and 400 °C, produce unstable devices with increasing positive shift for V_{ON} and a decrease in I_D. Higher temperature anneals, 600 and 800 °C, yield negligible changes in all parameters.

TFT instabilities are experimentally assessed as stress-induced changes in I_D, V_{ON}, and/or mobility as well as by the presence of hysteresis.

First, consider V_{ON} instability trends. V_{ON} corresponds to the gate voltage at which the drain current begins to flow. According to the discrete donor trap model, V_{ON} is a function of carrier concentration, as given by [31]

$$V_{ON} = \frac{-qt_{Channel}}{C_{Insulator}}\left(n_{co} - p_{to}\right), \tag{5.2}$$

where q is the charge, $t_{Channel}$ is the channel thickness, $C_{Insulator}$ is the capacitance per unit area of the gate oxide, n_{co} is the channel electron concentration in equilibrium (i.e., zero bias), and p_{to} is the empty trap concentration. Thus, according to this simple model, the magnitude of V_{ON} arises from a difference in the zero bias concentration of electrons present in the channel and the concentration of empty traps in the channel. However, this discrete donor trap model begs the question of the origin of these zero-bias concentrations, which are ultimately associated with charge present in the insulator and at the channel/insulator interface, and also with gate and channel work function differences [32]. Note that according to Eq. 5.2, V_{ON} can be either positive (enhancement-mode) or negative (depletion-mode), depending on the relative magnitudes of n_{co} and p_{to}. If V_{ON} is the only operative TFT instability, a

$\log(I_D)$-V_{GS} transfer curve would rigidly shift along the V_{GS}-axis, and perhaps increase or decrease along the I_D-axis, depending on gate leakage and/or the measurement noise floor.

Next, consider I_D and mobility stability trends. In a stability measurement, both of these quantities are monitored at gate voltages beyond threshold. Note that a stress-induced change in I_D at a constant overvoltage of V_{GS}-V_{ON} implies that the $\log(I_D)$-V_{GS} transfer curve changes in some type of non-rigid manner. Thus, the most complete method for assessing TFT stability is to monitor $\log(I_D)$-V_{GS} transfer curves as a function of stress time and to evaluate their rigid V_{ON} shifting and non-rigid I_D (subthreshold and above threshold) shifting trends.

Returning to I_D and mobility stability trends, at low electric field, a stress-induced change in drain current may be quantitatively described as

$$\Delta I_D = q\Delta n\Delta\mu\xi, \tag{5.1}$$

where q is the charge, Δn is the change in carrier concentration, $\Delta\mu$ is the change in carrier mobility, and ξ is the electric field. Thus, a change in drain current, ΔI_D, is due to a change in the carrier concentration, Δn, in the channel and/or a change in the mobility of the carriers present in the channel, $\Delta\mu$. It is usually the case that ΔI_D is dominated by a change in the carrier concentration, such that $\Delta I_D \approx q\Delta n\mu\xi$. It appears that the decrease seen in I_D for ZnO, ZIO, and IGO TFTs fabricated on thermal silicon oxide and annealed at 200 and 400 °C is associated primarily with a reduction in the carrier concentration. Additionally, the increase in I_D observed for the DC reactive sputtered ZnO TFT fabricated using spin-coat synthesized AlPO is attributed primarily to an increase in carrier concentration.

A stress-induced shift in V_{ON} can be ascribed to one of two possible mechanisms, trapping of carriers at the semiconductor/insulator or in the insulator, and/or mobile ion migration in the insulator. For the case of electron trapping in a n-channel TFT, when a positive voltage is applied to the gate (as shown in Fig. 5.19), negatively charged electrons may be trapped near the channel/insulator interface or be injected into the gate insulator from the semiconductor channel layer where they are trapped (Fig. 5.19(1)). The interface trapping and/or injection of electrons results in an increase in negative charge near the interface or in the insulator, thus leading to a positive shift in V_{ON}. Since only n-type materials

are considered in this work, hole injection into the insulator layer from the semiconductor is not applicable. The electron trapping mechanism is consistent with the shift in V_{ON} in the positive direction as seen in low temperature (200 and 400 °C) annealed TFTs fabricated on SiO_2.

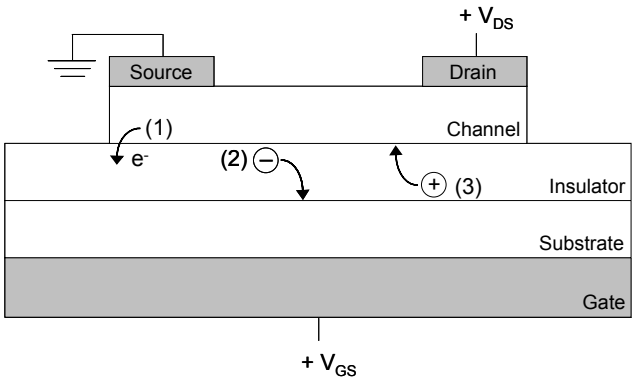

Figure 5.19: Cross-section of n-channel TFT subjected to a positive gate bias, showing (1) electron injection from the channel layer into the insulator and/or trapping near the channel/insulator interface, (2) negative mobile ion migration towards the insulator/gate interface, and (3) positive mobile ion migration towards the channel/insulator interface.

Migration of mobile ions in the insulator can also shift V_{ON} of a device. Under a positive applied gate bias, negatively (positively) charged mobile ions in the insulator tend to migrate to the insulator/gate interface (channel/insulator), as illustrated in Fig. 5.19(2) (Fig. 5.19(3)). Mobile ions have the greatest effect on V_{ON} at the channel/insulator interface, and no effect when they are at the insulator/gate interface. Thus, as V_{ON} decreases (increases), negatively (positively) charge mobile ions move away from the channel/insulator (insulator/gate) interface. The negative shift in V_{ON} observed in the DC reactive sputtered ZnO TFT fabricated on an AlPO gate dielectric is consistent with the movement of negatively charged mobile ions in the insulator. The positive shift in the other ZnO, ZIO, and IGO TFTs fabricated using SiO_2 is attributed to electron trapping, rather than to positively charged mobile ions for several reasons. Thermal silicon oxide is a very robust dielectric; thus it would be unlikely for instabilities to be present in the insulator. Also positive mobile ions drift is inconsistent with hysteresis trends (as discussed below).

As briefly discussed in Section 5.2.1, instabilities can be categorized as reversible or irreversible with an extended period of rest (i.e., 30 days). At the outset of this research project, it was hypothesized that an ionic drift mechanism in the insulator would be irreversible, whereas electron trapping near the channel/insulator interface would be reversible with respect to rest. However, if electrons are trapped into energetically and/or spatially remote traps so that this trapping is persistent, it is possible that this trapping would appear to be reversible with respect to an extended rest. In order to more accurately assess the extent of reversibility, a more aggressive testing methodology would be required, such as the application of an intense light source or and elevated temperature so that electron de-trapping occurs. It is contended that if assertive trap resetting measures are employed, it will be found that mobile ion migration mechanism gives rise to irreversible instabilities while electron trapping is reversible.

TFT instabilities are often manifested as hysteresis in I_D curves measured as a function of a continuous sweep of either V_{DS} or V_{GS} in both a positive and negative sweep direction. Hysteresis can either be clockwise and counter-clockwise. As illustrated in Fig. 5.20, hysteresis may be quantified as a change in the turn-on voltage of a continuously swept curve. A stress-induced change in V_{ON} may be expressed as

$$\Delta V_{ON} = \frac{-\Delta\gamma Q}{C_{insulator}}, \tag{5.3}$$

where Q is the charge per unit area which rearranges and thus gives rise to hysteresis, γ is the charge centroid of the rearranged charge giving rise to a hysteresis, normalized to the insulator thickness, and $C_{insulator}$ is the capacitance per unit area of the gate insulator. The charge rearrangement, Q, can either be positive for positive charge (holes and positive mobile ions) or negative for negative charge (electrons and negative mobile ions). The centroid can have a value between 0 and 1, i.e. $0 \leq \gamma \leq 1$. $\gamma = 0$ if all of the rearranged charge is located at the insulator/gate interface, and $\gamma = 1$ if all of the rearrange charge is located at the channel/insulator interface. $\Delta\gamma$ can also either be positive or negative; positive for charge moving toward the channel/insulator interface, and negative for charge moving toward the insulator/gate interface.

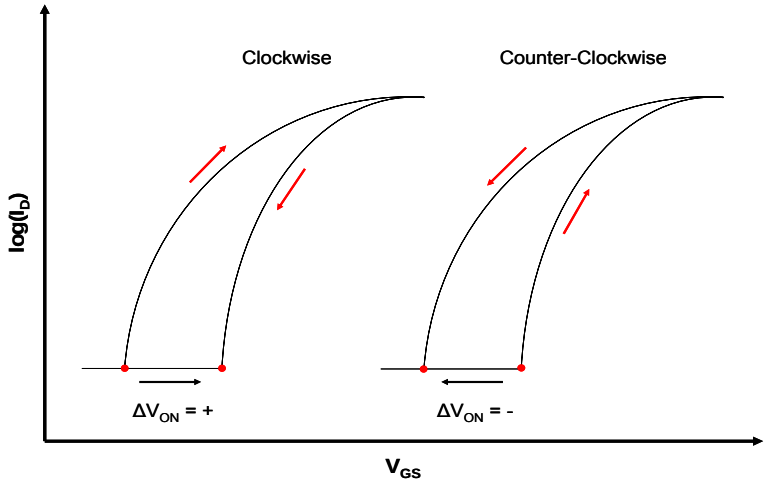

Figure 5.20: $\log(I_D)$-V_{GS} plot showing clockwise and counter-clockwise hysteresis. Clockwise hysteresis manifests a positive shift in V_{ON} while counter-clockwise hysteresis results in a negative shift in V_{ON}.

Equation 5.3 can be used to explain the shifts in V_{ON} related to hysteresis, as summarized in Table 5.16. A positive shift in V_{ON} due to clockwise hysteresis is attributed to a positive change in $\Delta\gamma$ and a negative charge rearrangement. A negative shift in V_{ON} due to counter-clockwise hysteresis is attributed to either a positive change in $\Delta\gamma$ and a positive charge rearrangement, or to a negative change in $\Delta\gamma$ and a negative charge arrangement.

Hysteresis	$\Delta\gamma$	Q	ΔV_{ON}
Clockwise	+	– (electron trapping)	+
Counter-clockwise	+	+ (positive mobile ions)	–
Counter-clockwise	–	– (negative mobile ions)	–

Table 5.17: Summary of hysteresis trends as manifested as a change in V_{ON} for an n-channel TFT, in which the polarity of the gate voltage is positive.

Clockwise hysteresis is observed in TFTs annealed at 200 °C for ZnO, ZIO, and IGO fabricated on thermal silicon oxide. The low temperature instabilities seen are primarily due to the quality of the channel layer, as higher temperatures exhibit negligible or no hysteresis. Since clockwise hysteresis manifests a positive shift in V_{ON}, it can inferred from Eq. 5.3 and Table 5.7, that Q is negative, most likely due to electrons, and that $\Delta\gamma$ is positive due to electron trapping in deep level traps in the channel and/or near the insulator/channel interface. Counter-clockwise hysteresis is observed in a reactively sputtered ZnO TFT fabricated on spin coat synthesized AlPO as the gate insulator and annealed at 600 °C. In this device, the instabilities are primarily due to the poor quality of the insulator, as it is known that higher channel annealing temperature results in higher quality channels when a robust thermal silicon oxide gate insulate is used. Based on Eq. 5.3 and Table 5.7, there are two possible mechanisms for to explain counter-clockwise hysteresis. First, that the negative shift in V_{ON} is associated with positive charge, where Q is positive due to positive mobile ions and $\Delta\gamma$ is positive due to positive mobile ions moving towards the channel/insulator interface. The second possibility is due to negative charge migration. Q is negative due to negative mobile ions and $\Delta\gamma$ is negative due to negative mobile ions moving toward the insulator/gate interface. It cannot be determined which of these mechanisms causes the negative shift in V_{ON}.

In summary, as shown in Table 5.18, it is found that the ZnO TFT fabricated using AlPO as the gate dielectric possesses a negative shift in V_{ON} and counter-clockwise hysteresis. It cannot yet be determined which type of mobile ion charge, positive or negative, gives rise to these trends. Chemists working on this project believe that it is positively charged proton migration in the insulator is the most likely explanation [33]. Experimental results also indicate that a higher temperature at 1000 °C leads to a robust insulator [33]. All of the TFTs using a thermal silicon oxide gate insulator yield a positive shift in V_{ON} and concomitant clockwise hysteresis, which is attributed to electron trapping near the channel/insulator interface.

Material System	ΔV_{ON}	Hysteresis	Mechanism
ZnO/AlPO	Negative	Counter-clockwise	Positive mobile ions or Negative mobile ions
ZnO/SiO2 ZIO/SiO2 IGO/SiO2	Positive	Clockwise	Electron trapping

Table 5.18: Summary of TFT instability trends and their proposed mechanisms.

5.3 Conclusion

A methodology developed for assessing the stability of oxide-based TFTs is implemented. Stability criteria: shifting in V_{ON}, a change I_D, a change in the peak channel mobility, and also the presence of hysteresis are investigated and the stability of ZnO, ZIO, and IGO TFTs are determined. It is found that TFTs with a robust thermal silicon oxide gate insulator are stable after a higher post-deposition anneal temperature i.e., 600-800 °C, with the exception of ZIO, which is stable at 400 °C. Also, TFTs fabricated using SiO_2 as a gate dielectric and annealed at 200 and 400 °C are unstable. This instability manifests as a positive shift in V_{ON} and clockwise hysteresis in the initial $\log(I_D)$-V_{GS} transfer curve obtained at zero stress time. Such instabilities are attributed to electron trapping. In contrast, the ZnO TFT fabricated on an AlPO gate dielectric is also unstable but possesses a negative shift in V_{ON} and counter-clockwise hysteresis, which is ascribed to electron trapping at the channel/insulator interface or within the channel.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

This thesis focuses on two aspects of oxide-based thin-film transistors (TFTs), contact resistance and instability assessment. Conclusions related to these two areas are summarized as follows.

First, determination of the contact resistance of indium tin oxide (ITO) on two wide-band gap semiconductors, zinc oxide (ZnO) and indium gallium oxide (IGO) is attempted and the effects of contact resistance on device performance is investigated. Both transistor and transfer length method (TLM) structures are used in the study and three material systems are employed: ZnO on SiO_2, ZnO on aluminum titanium oxide (ATO), and IGO on SiO_2. It is found that the measured resistance is not dominated by contact resistance effects. However, it is unclear whether the contact resistance is a negligible or a small effect since the indeterminate nature of the data is due largely to data variability. It is likely that smaller device dimension will reduce the data variability. The contact resistance extracted from ZnO/SiO2 TFTs and ZnO/ATO TFTs is ~ 0 and 0.7-3 kΩ-cm, respectively. This suggests that the dielectric material plays a role in determining the contact resistance as reactions may be taking place at the channel/insulator interface. It is also noted that the surface roughness for thermal silicon oxide is ~ 0.28 nm, while ATO is ~ 5.5 nm. This difference in surface roughness may contribute to the difference in contact resistance. Moreover, it is concluded that the device dimensions used in this study are too large to yield an accurate estimate of the contract resistance.

Second, a methodology for assessing the stability of oxide-based TFTs is developed and implemented. This methodology involves constant voltage stressing over a maximum duration of 105 s (i.e., ~ 28 hours) and periodic evaluation of drain current-drain voltage and drain current-gate voltage characteristics during the stability test. This stability assesment strategy is first applied to three semiconducting materials: ZnO, zinc indium oxide (ZIO), and IGO, using thermal silicon oxide as the gate dielectric and similar trends are observe. Relatively stable devices are obtained for post-deposition anneal temperatures of ~ 600 °C for ZnO and IGO TFTs, and ~ 400 °C for ZIO TFTs. The presence of

instabilities result in a positive shift in the turn-on voltage and clockwise hysteresis in the drain current-gate voltage transfer curves. Such instabilities are attributed to electron trapping near the channel/insulator interface. The stability a ZnO TFT fabricated using a spin-coat synthesized aluminum phosphate (AlPO) as the gate dielectric is also investigated. The ZnO/AlPO TFT showed distinctively different stability trends. This device is observed to be very unstable with a negative shift in the turn-on voltage and the presence of counter-clockwise hysteresis. Mechanisms for these instabilities are ascribed to insulator ion drift. It is shown that stable TFTs can be fabricated with oxide-based channel layers if a high quality insulator is available and if a post-deposition anneal at elevated temperatures is employed.

6.2 Recommendations for future work

The work in this thesis has brought about many questions that have been left unexplored and unanswered. The purpose of this section is to summarize directions for further research based on the findings presented in this thesis.

Since the device dimensions used in this work are relatively large, smaller dimensions are needed to properly determine the contact resistance and the effect of contact resistance on device performance. For example, Luan and Neudeck obtained results using a channel length ranging from 0.5 to 40 μm for TFTs and TLM contact spacing of 1, 2, 4, 8, and 16 μm [17]. Other suggested work includes automation of data collection and contact resistance related device modeling.

The work assessing TFT stability in this thesis qualifies as a foundation for future research. The main purpose is to demonstrate the viability of the stability assessment methodology. Future research should involve automating data collection, further development of the characterization technique, investigation of instability mechanisms, and an exploration of instability reversibility/irreversibility. Ideas used to determine a-Si:H TFTs instability mechanisms include reverse polarity biasing and immersion in a salt solution [24,34]. Another idea would be to induce energy into the semiconductor layer via temperature or a light source, such as UV, in an attempt to

rigorously reset electron traps so that the instabilities may be classified as reversible or irreversible [35]. Another suggestion for future work is to explore the temperature dependence of instabilities [36].

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